

Service
Service
Service

DVDR3355/02/05/19/51 & DVDR3365/02/05/19/51



Back End Repair

Service Manual



Contents	Page
1 Technical Specifications and Connection Facilities	2
2 Safety Information, General Notes & Lead Free Requirements	5
3 Directions for Use	7
4 Mechanical Instructions	9
5 Upgrade Software & Repair Chart	12
6 Block Diagrams, Waveforms, Wiring Diagram	19
Overall block diagram	19
Control block diagram	20
Wiring diagram	21
Waveforms of Analog Board	22
Waveforms of Digital Board	23
Test Point Overview for Analog Board	24
Test Point Overview for Digital Board	25
7 Circuit Diagram and PWB Layout	26
Analog: Frontend Video (FV)	26
Analog: Video In / Out (IOV)	27
Analog: Audio In / Out (IOA)	28
Analog: Power Supply (PS)	29
Analog: Multi Sound Processing (MSP)	30
Analog: Audio Converter (DAC_ADC)	31
Analog: Digital In / Out 1 (DIGIO 1)	32
Layout: Analog-Main Part (Top View)	33
Layout: Analog-Main Part (Bottom View)	34
Front: Front Panel	35

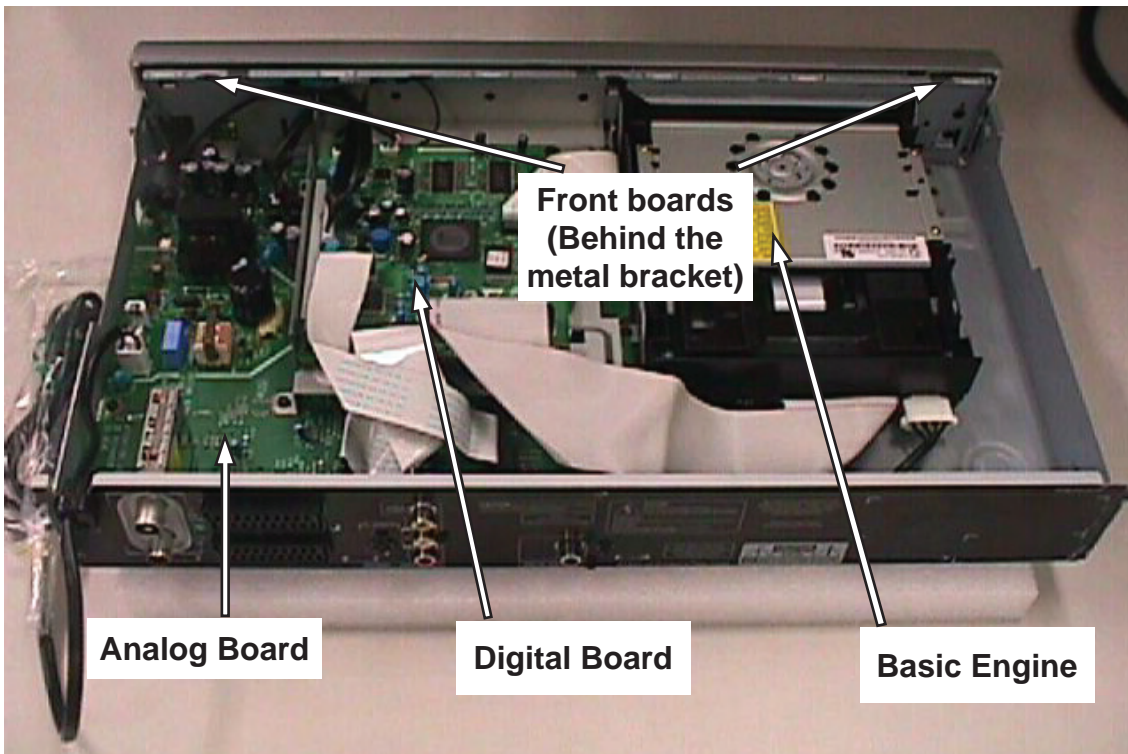
Contents	Page
Front: Front Panel	36
Layout: Front Panel (Top View)	37
Front: Standby	38
Layout: Standby (Top View)	38
Digital: Back-end Processor	39
Digital: Memory	40
Digital: IEEE 1394 Physical Layer	41
Digital: Video Input Processor	42
Digital: Interfaces	43
Layout: Digital-Main Part (Top View)	44
Layout: Digital-Main Part (Bottom View)	45
8 Circuit- and IC Description	47
Front Board (Panel – Display + Key)	47
Analog Board	47
Digital Board	52
IC Description	55
Analog Board	55
Digital Board	60
9 Exploded View & Spare Parts List	71
Exploded View of the set	71
Spare Parts List	72
10 Revision List	73

©Copyright 2005 Philips Consumer Electronics B.V. Eindhoven, The Netherlands.
All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted, in any form or by any means, electronic, mechanical, photocopying, or otherwise without the prior permission of Philips.



1. Technical Specifications and Connection Facilities

1.1 PCB Locations



1.2 General:

Mains voltage	: 220V – 240V
Mains frequency	: 50 Hz
Power consumption (typical)	: 25 W
Standby Power Consumption	: < 4 W

1.3 RF Tuner

Test equipment: Fluke 54200 TV Signal generator
Test streams: PAL BG Philips Standard test pattern

1.3.1 System

PAL B/G, PAL D/K, SECAM L/L', PAL I

1.3.2 RF - Loop Through:

Frequency range	: 45 MHz – 860 MHz
Gain: (ANT IN - ANT OUT)	: -6dB to 0dB

1.3.3 Receiver:

PLL tuning with AFC for optimum reception	
Frequency range	: 45.25 MHz – 857 MHz
Sensitivity at 40dB S/N	: $\geq 60\text{dB}\mu\text{V}$ at 75 Ω (video unweighted)

1.3.4 Video Performance:

Channel 25 / 503,25 MHz,	
Test pattern: PAL BG PHILIPS standard test pattern,	
RF Level 74dBV	
Measured on SCART 1	
Frequency response	: 0.1 – 4.00 MHz \pm 3dB
Group delay (0.1 MHz - 4.4 MHz)	: 0 nsec \pm 150 nsec

1.3.5 Audio Performance:

Audio Performance Analogue - HiFi:

Frequency response at SCART 1 (L+R) output	: 100 Hz – 12 kHz / 0 \pm 3dB
S/N according to DIN 45405, 7, 1967 and PHILIPS standard test pattern video signal	: $\geq 50\text{dB}$, unweighted
Harmonic distortion (1 kHz, ± 25 kHz deviation)	: $\leq 1.5\%$

Audio Performance NICAM:

Frequency response at SCART 1 (L+R) output	: 40 Hz – 15 kHz / 0 \pm 3dB
S/N according to DIN 45405,7,1967 and PHILIPS standard test pattern video signal	: $\geq 60\text{dB}$, unweighted
Harmonic distortion (1kHz)	: $\leq 0.5\%$

1.3.6 Tuning

Automatic Search Tuning

Scanning time without antenna	: typ. 3 min.
Stop level (vision carrier)	: $\geq 37\text{dB}\mu\text{V}$
Maximum tuning error of a recalled program	: $\pm 62.5\text{ kHz}$
Maximum tuning error during operation	: $\pm 100\text{ kHz}$

Tuning Principle

Automatic B, G, I, DK and L/L' detection
Manual selection in "STORE" mode

1.4 Analogue Inputs / Outputs

1.4.1 SCART 1 (Connected to TV)

Pin Signals:

1 - Audio R	1.8V RMS
2 - Audio R	
3 - Audio L	1.8V RMS
4 - Audio GND	
5 - Blue / GND	
6 - Audio L	
7 - Blue out	
8 - Function switch	< 2V = TV > 4.5V / < 7V = asp. Ratio 16:9 DVD > 9.5V / < 12V = asp. Ratio 4:3 DVD
9 - Green GND	
10 - NC	
11 - Green	0.7Vpp \pm 0.1V into 75 Ω (*)
12 - NC	
13 - Red GND	
14 - Fast switch GND	
15 - Red out	0.7Vpp \pm 0.1V into 75 Ω (*)
16 - Fast switch RGB / CVBS	< 0.4V into 75 Ω = CVBS >1V / < 3V into 75 Ω = RGB
17 - CVBS GND OUT	
18 - CVBS GND IN	
19 - CVBS out	1Vpp \pm 0.1V into 75 Ω (*)
20 - CVBS in	
21 - Shield	

1.4.2 SCART 2 (Connected to AUX)

Pin Signals:

1 - Audio R	1.8V RMS
2 - Audio R	
3 - Audio L	1.8V RMS
4 - Audio GND	
5 - Blue GND	
6 - Audio L	
7 - Blue in	
8 - Function switch	
9 - Green GND	
10 - NC	
11 - Green in	
12 - NC	
13 - Red GND	
14 - Fast switch GND	
15 - Red in	
16 - Fast switch RGB / CVBS	
17 - CVBS GND OUT	
18 - CVBS GND IN	
19 - CVBS / RGB out sync	1Vpp \pm 0.1V into 75 Ω (*)
20 - CVBS in	
21 - Shield	

(*) for 100% white

1.4.3 Audio/Video Front Input Connectors

Audio - Cinch

Input voltage	: 2.2Vrms
Input impedance	: > 10k Ω

Video - Cinch

Input voltage	: 1Vpp \pm 3dB
Input impedance	: 75 Ω

Video - YC (Hosiden)

According to IEC 933-5

Superimposed DC-level on pin 4 (load > 100k Ω)

< 2.4V is detected as 4:3 aspect ratio

> 3.5V is detected as 16:9 aspect ratio

Input voltage Y	: 1Vpp \pm 3dB
Input impedance Y	: 75 Ω
Input voltage C	: burst 300mVpp \pm 3dB
Input impedance C	: 75 Ω

1.4.4 Audio/Video Output rear Connectors

Audio - Cinch

Output voltage	: 2Vrms max.
Output impedance	: > 10k Ω

Video - Cinch

Output voltage	: 1Vpp \pm 3dB
Output impedance	: 75 Ω

Video - YC (Hosiden)

According to IEC 933-5

Superimposed DC-level on pin 4 (load > 100k Ω)

< 2.4V is detected as 4:3 aspect ratio

> 3.5V is detected as 16:9 aspect ratio

Output voltage Y	: 1Vpp \pm 10/-15%
Output voltage C	: 300mVpp \pm 1/-4dB

1.5 Video Performance

All outputs loaded with 75 Ω

SNR measurements over full bandwidth without weighting.

1.5.1 SCART (RGB)

SNR	: > -65dB on all output
Bandwidth	: 4.8MHz \pm 2dB

1.6 Audio Performance CD

1.6.1 Cinch Output Rear

Output voltage 2 channel mode	: 2Vrms \pm 2dB
Channel unbalance (1kHz)	: < 1dB
Crosstalk 1kHz	: > 95dB
Crosstalk 16Hz-20kHz	: > 87dB
Frequency response 20Hz-20kHz	: \pm 0.2dB max
Signal to noise ratio	: > 85dB
Dynamic range 1kHz	: > 83dB
Distortion and noise 1kHz	: > 83dB
Distortion and noise 16Hz-20kHz	: > 75dB
Intermodulation distortion	: > 70dB
Mute	: > 95dB
Outband attenuation:	: > 40dB above 30kHz

1.6.2 Scart Audio

Output voltage 2 channel mode	: 1.6Vrms ± 2dB
Channel unbalance (1kHz)	: < 1dB
Crosstalk 1kHz	: > 85dB
Crosstalk 16Hz-20kHz	: > 70dB
Frequency response 20Hz-20kHz	: ± 0.2dB max
Signal to noise ratio	: > 80dB
Dynamic range 1kHz	: > 75dB
Distortion and noise 1kHz	: > 75dB
Distortion and noise 16Hz-20kHz	: > 50dB
Intermodulation distortion	: > 70dB
Mute	: > 80dB
Outband attenuation:	: > 40dB above 25kHz

1.7 Digital Output

1.7.1 Coaxial

CDDA / LPCM (incl MPEG1)	: according IEC958, IEC60958-1,-3
MPEG2, AC3 audio	: according IEC1937, IEC61937
DTS	: according IEC1937, IEC 61937 amendment 1

1.8 Digital Video Input (IEEE 1394)

1.8.1 Applicable Standards

Implementation according:
 IEEE Std 1394-1995
 IEC 61883 - Part 1
 IEC 61883 - Part 2 SD-DVCR (02-01-1997)

Specification of consumer use digital VCR's using 6.3 mm
 magnetic tape - dec. 1994
 Annex A of 61883-1

1.9 Dimensions and Weight

Height of feet	: 5.5mm
Apparatus tray closed	: WxDxH:435x285x65mm
Apparatus tray open	: WxDxH:435x422x65mm
Weight without packaging	: app. 4.0kg ± 0.5kg
Weight with packaging	: app. 6kg

1.10 Laser Output Power & Wavelength

1.10.1 DVD

Output power during reading	: 0.8mW
Output power during writing	: 20mW
Wavelength	: 660nm

1.10.2 CD


Output power	: 0.3mW
Wavelength	: 780nm

2. Safety Information, General Notes & Lead Free Requirements

2.1 Safety Instructions

2.1.1 General Safety

Safety regulations require that during a repair:

- Connect the unit to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol , only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that after a repair, you must return the unit in its original condition. Pay, in particular, attention to the following points:

- Route the wires/cables correctly, and fix them with the mounted cable clamps.
- Check the insulation of the mains lead for external damage.
- Check the electrical DC resistance between the mains plug and the secondary side:
 1. Unplug the mains cord, and connect a wire between the two pins of the mains plug.
 2. Set the mains switch to the 'on' position (keep the mains cord unplugged!).
 3. Measure the resistance value between the mains plug and the front panel, controls, and chassis bottom.
 4. Repair or correct unit when the resistance measurement is less than 1 MΩ.
 5. Verify this, before you return the unit to the customer/user (ref. UL-standard no. 1492).
 6. Switch the unit 'off', and remove the wire between the two pins of the mains plug.

2.1.2 Laser Safety

This unit employs a laser. Only qualified service personnel may remove the cover, or attempt to service this device (due to possible eye injury).

Laser Device Unit

Type	: Semiconductor laser GaAlAs
Wavelength	: 650 nm (DVD) 780 nm (VCD/CD)
Output Power	: 20 mW (DVD+RW writing) 0.8 mW (DVD reading) 0.3 mW (VCD/CD reading)
Beam divergence	: 60 degree




Figure 2-1

Note: Use of controls or adjustments or performance of procedure other than those specified herein, may result in hazardous radiation exposure. Avoid direct exposure to beam.

2.2 Warnings

2.2.1 General

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD, ). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are at the same potential as the mass of the set by a wristband with resistance. Keep components and tools at this same potential. Available ESD protection equipment:
 - Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
 - Wristband tester 4822 344 13999.
- Be careful during measurements in the live voltage section. The primary side of the power supply, including the heatsink, carries live mains voltage when you connect the player to the mains (even when the player is 'off!'). It is possible to touch copper tracks and/or components in this unshielded primary area, when you service the player. Service personnel must take precautions to prevent touching this area or components in this area. A 'lightning stroke' and a stripe-marked printing on the printed wiring board, indicate the primary side of the power supply.
- Never replace modules, or components, while the unit is 'on'.

2.2.2 Laser

- The use of optical instruments with this product, will increase eye hazard.
- Only qualified service personnel may remove the cover or attempt to service this device, due to possible eye injury.
- Repair handling should take place as much as possible with a disc loaded inside the player.
- Text below is placed inside the unit, on the laser cover shield:

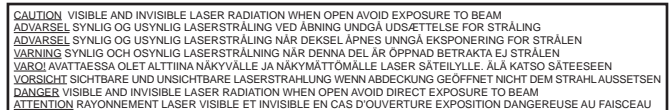


Figure 2-2

2.2.3 Notes

Dolby

Manufactured under licence from Dolby Laboratories. "Dolby", "Pro Logic" and the double-D symbol are trademarks of Dolby Laboratories. Confidential Unpublished Works. ©1992-1997 Dolby Laboratories, Inc. All rights reserved.



Figure 2-3

Trusurround

TRUSURROUND, SRS and symbol (fig 2-4) are trademarks of SRS Labs, Inc. TRUSURROUND technology is manufactured under licence from SRS labs, Inc.



Figure 2-4

Video Plus

"Video Plus+" and "PlusCode" are registered trademarks of the Gemstar Development Corporation. The "Video Plus+" system is manufactured under licence from the Gemstar Development Corporation.



Figure 2-5

Macrovision

This product incorporates copyright protection technology that is protected by method claims of certain U.S. patents and other intellectual property rights owned by Macrovision Corporation and other rights owners.

Use of this copyright protection technology must be authorized by Macrovision Corporation, and is intended for home and other limited viewing uses only unless otherwise authorized by Macrovision Corporation. Reverse engineering or disassembly is prohibited.

2.3 Lead Free Requirement**Information about Lead-free produced sets**

Philips CE is starting production of lead-free sets from 1.1.2005 onwards.

INDENTIFICATION:

Regardless of special logo (not always indicated)



One must treat all sets from **1 Jan 2005** onwards, according next rules.

Example S/N:



Bottom line of typeplate gives a 14-digit S/N. Digit 5&6 is the year, digit 7&8 is the week number, so in this case 1991 wk 18

So from 0501 onwards = from 1 Jan 2005 onwards

Important note: In fact also products of year 2004 must be treated in this way as long as you avoid mixing solder-alloys (lead/ lead-free). So best to always use SAC305 and the higher temperatures belong to this.

Due to lead-free technology some rules have to be respected by the workshop during a repair:

- Use only lead-free solder alloy Philips SAC305 with order code 0622 149 00106. If lead-free solder-pate is required, please contact the manufacturer of your solder-equipment. In general use of solder-paste within workshops should be avoided because paste is not easy to store and to handle.
- Use only adequate solder tools applicable for lead-free solder alloy. The solder tool must be able
 - To reach at least a solder-temperature of 400°C,
 - To stabilize the adjusted temperature at the solder-tip
 - To exchange solder-tips for different applications.
- Adjust your solder tool so that a temperature around 360°C – 380°C is reached and stabilized at the solder joint. Heating-time of the solder-joint should not exceed ~ 4 sec. Avoid temperatures above 400°C otherwise wear-out of tips will rise drastically and flux-fluid will be destroyed. To avoid wear-out of tips switch off un-used equipment, or reduce heat.
- Mix of lead-free solder alloy / parts with leaded solder alloy / parts is possible but PHILIPS recommends strongly to avoid mixed solder alloy types (leaded and lead-free). If one cannot avoid or does not know whether product is lead-free, clean carefully the solder-joint from old solder alloy and re-solder with new solder alloy (SAC305).
- Use only original spare-parts listed in the Service-Manuals. Not listed standard-material (commodities) has to be purchased at external companies.
- **Special information for BGA-ICs:**
 - always use the 12nc-recognizable soldering temperature profile of the specific BGA (for de-soldering always use the lead-free temperature profile, in case of doubt)
 - lead free BGA-ICs will be delivered in so-called 'dry-packaging' (sealed pack including a silica gel pack) to protect the IC against moisture. After opening, dependent of MSL-level seen on indicator-label in the bag, the BGA-IC possibly still has to be baked dry. (MSL=Moisture Sensitivity Level). This will be communicated via AYS-website.
- Do not re-use BGAs at all.
- For sets produced before 1.1.2005 (except products of 2004), containing leaded solder-alloy and components, all needed spare-parts will be available till the end of the service-period. For repair of such sets nothing changes.
- On our website www.atyourservice.ce.Philips.com you find more information to:
 - BGA-de-/soldering (+ baking instructions)
 - Heating-profiles of BGAs and other ICs used in Philips-sets

You will find this and more technical information within the "magazine", chapter "workshop news".

For additional questions please contact your local repair-helpdesk.

3. Directions For Use

The following excerpt of the Quick Use Guide serves as an introduction to the set.

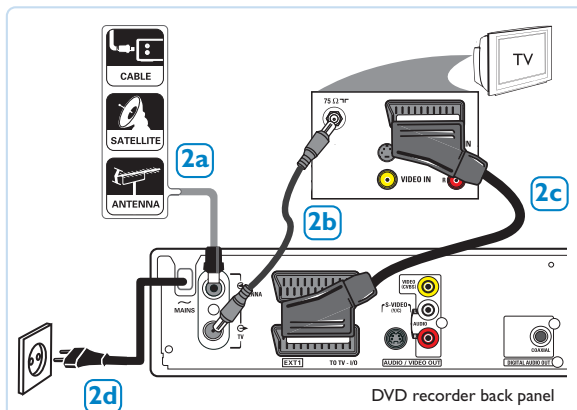
The Complete Direction for the Use can be downloaded in different languages from the internet site of Philips Customer care Center: www.p4c.philips.com

QUICK START GUIDE

1 what's in the box



2 connect DVD recorder



2a Connect existing antenna cable/satellite signal (or from the Cable/Satellite Box [RF OUT or TO TV]) to the **ANTENNA** input socket at the back of the DVD recorder.

2b Use the supplied RF coaxial cable to connect the DVD recorder's **VIDEO IN** output socket to your TV's antenna input socket.

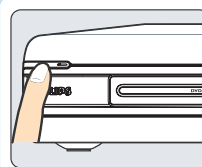
2c Use the supplied Scart cable to connect the DVD recorder's **EXT 1 TO TV-I/O** socket to the matching SCART input socket at the back of your TV.

2d Connect the power cable from the DVD recorder's ~ **MAINS** to the AC power outlet.

Helpful Hint:

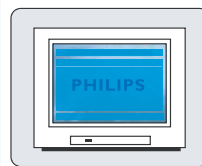
For additional connection diagrams, see User Manual pages 12~19.

3 Start initial setup

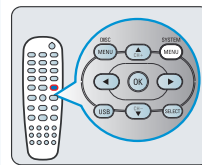


3a Press **STANDBY-ON** on the DVD recorder to turn it on.

Note: For successful installation, your cable/satellite box must be turned on.

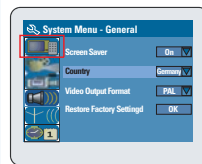


3b Turn on the TV to the correct programme channel for the input socket ('EXT', '0', 'AV').
→ The blue PHILIPS DVD background screen will appear on the TV.



3c Press **SYSTEM MENU** on the remote control.

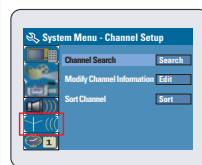
→ Use **▲▼** keys to go through the menu. Select an item by pressing **▶**, and confirm a setting by pressing **OK**.



3d Highlight **Country** and press **▶**.

Select the **country of your residence**.

Select **{ Country }** and press **OK** on the remote control.



3e Highlight **Channel Search** and press **▶**.

Setup and install **TV channels**.

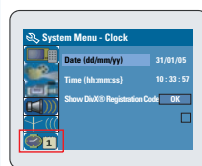
Select **{ Channel Search }** and press **OK** on the remote control to start automatic TV channel search.



3f Highlight **On-Screen Display Language** and press **▶**.

Select the **language**.

- select TV On-Screen Display language.
- select default Disc Menu language.
- select default subtitle language.
- select default audio language.



3g Highlight **Date** and **Time** and press **▶**.

Set the **Date and Time**.

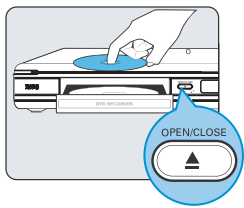
Use the **numeric keypad 0-9** to input the date/time, then press **OK** to confirm.

3h Press **SYSTEM MENU** to exit.

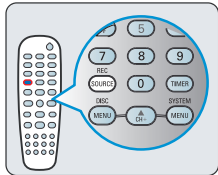
The DVD recorder is ready for use!

See next page for basic recording and playback.

4 start manual recording

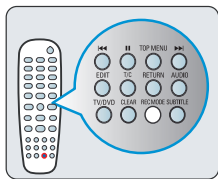


- 4a** Insert a recordable DVD+R/+RW with the label facing up.



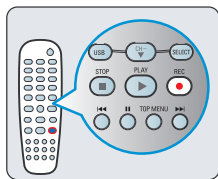
- 4b** To record TV programme, press **REC SOURCE** to select {Tuner}.

To record from an external device connected to this DVD Recorder, press **REC SOURCE** repeatedly to select the corresponding external input channel : { Front CVBS } { Front S-Video }, { DV }, { EXT 2 }.

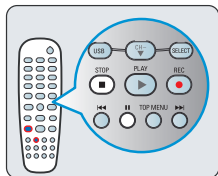


- 4c** Press **REC MODE** to select a desired recording mode. It defines the picture quality and the maximum recording time for a disc.

Maximum Recording Time per Disc	Picture Quality	Record Mode
1 hour	High quality	1 Hour Mode
2 hours	DVD quality-Standard Play	2 Hour Mode
4 hours	VHS quality-Extended Play	4 Hour Mode
6 hours	VHS quality-Super Long Play	6 Hour Mode



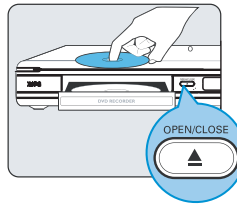
- 4d** Press **REC** to start recording.



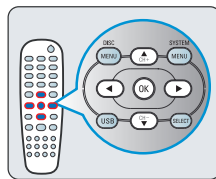
- 4e** To pause the recording, press **II**. To resume recording, press **REC**.

To stop the recording, press **STOP**.
→ Wait until the message disappears from the display panel before you remove the disc.

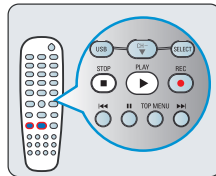
5 start playback



- 5a** Insert a disc with the label side facing up.

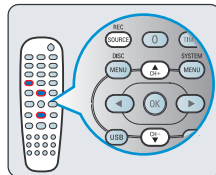


- 5b** Playback may start automatically. If not, press **PLAY**.
→ If a disc menu appears, use **◀▶▲▼** keys to navigate within the menu, highlight a title and press **OK** to start playback.



- 5c** To stop playback, press **STOP**.

To watch the TV programmes



- 5d** Press **REC SOURCE** to select {Tuner}, then use **▲▼** keys to select the programme number.

GET PICTURE

- Check the AV mode on TV. It may be called FRONT, A/V IN, or VIDEO. Choose the different modes using TV remote control.
- Or, use the TV remote control to select Channel 1 on TV, then press Channel down button until you get the picture.
- See your TV manual for more details.

GET SOUND

- Use the supplied scart cable to connect the DVD recorder to your TV, the picture and sound will output through the TV.
- Or, connect the AUDIO L/R (red/white) sockets at the back of the DVD recorder to the corresponding AUDIO input sockets on a TV, stereo system or receiver. Turn on the connected system and select the appropriate channel.

4. Mechanical Instructions

4.1 Dismantling and Assembly of the Set

For item numbers please see the exploded view in Chapter 9.

4.1.1 Dismantling of the DVD Loader Tray Cover

- 1) Inserting a minus screw driver and push the lever in the direction as shown in Figure 4-1 to unlock the tray before sliding it out.

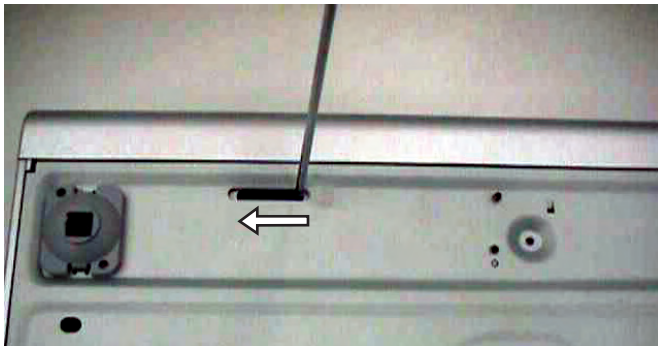


Figure 4-1

- 2) Remove the Tray Cover as shown in Figure 4-2.



Figure 4-2

4.1.2 Dismantling of the Front Panel Assembly

- 1) Remove the 3 screws 188 and release the 2 snap hooks on the side before removing the front assembly.

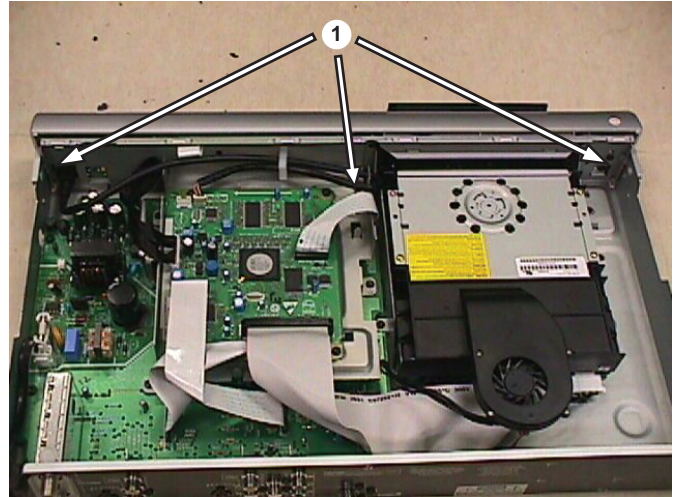


Figure 4-3

- 2) Remove the 5 screws 186 to remove the front plate 184 as shown in Figure 4-4.

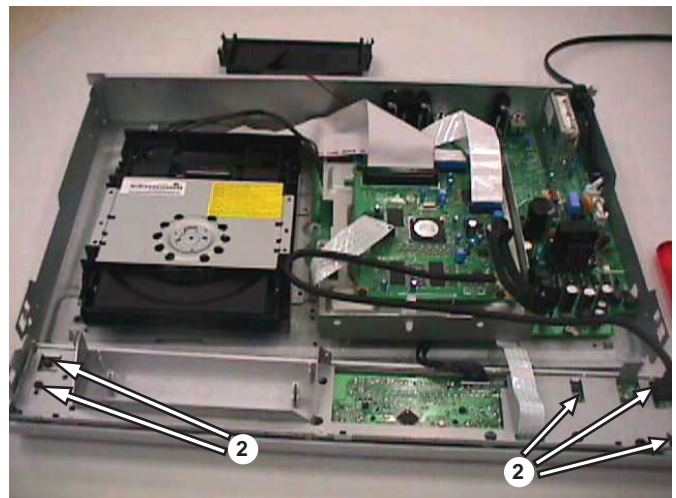


Figure 4-4

4.1.3 Dismantling of the Basic Engine

- 1) Remove the Cover Tray (See 4.1.1).
- 2) Remove the 4 screws 260 to free the Basic Engine.

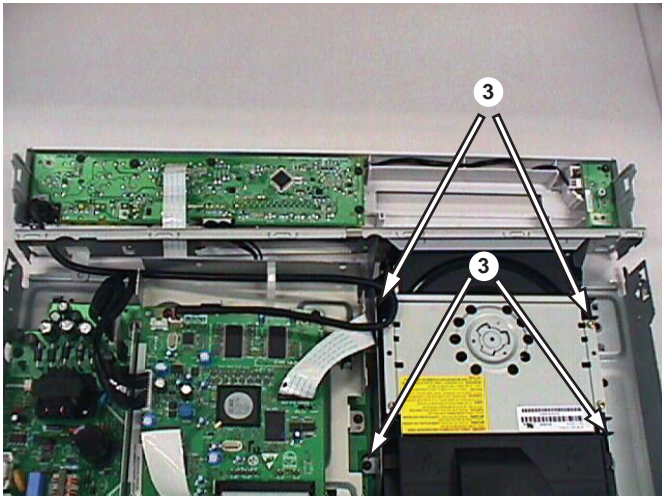


Figure 4-5

- 3) Place the Basic Engine in the service position by flipping the basic engine to the vertical position

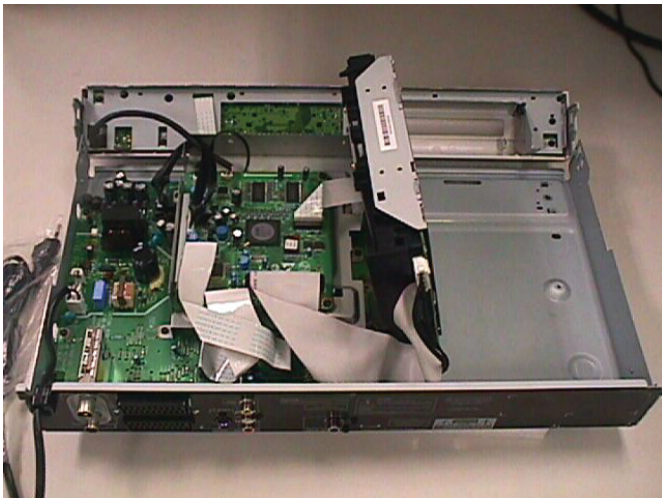


Figure 4-6

4.1.4 Dismantling of the Digital Board

- 1) Remove the 4 screws 272 to loose the Digital Board as shown in Figure 4-7.

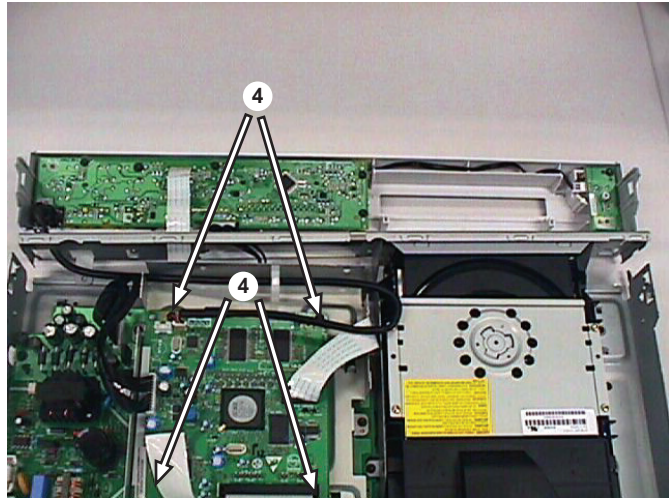


Figure 4-7

- 2) Service Position can be achieved by flipping the Digital board to the Vertical Position as shown in Figure 4-8.

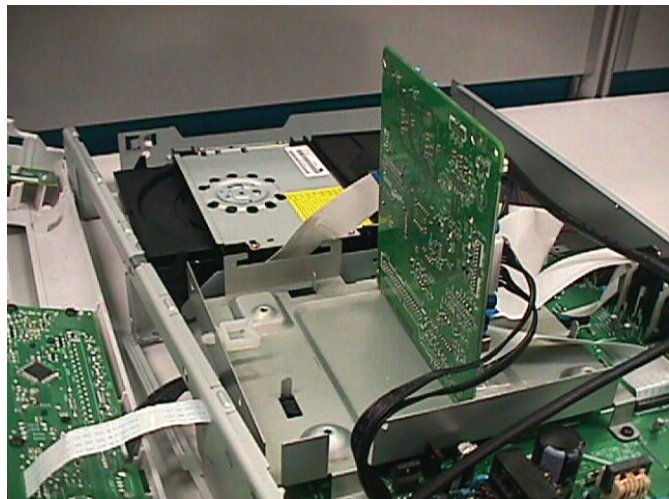


Figure 4-8

Note: The cable (just to transfer the service connection to the analog board) from socket 1101 can be removed and use for hyperterminal connection.

4.1.5 Dismantling of the Analog Board

- 1) Remove 5 screws 244 and 4 screws 252 and screw 230.
- 2) Remove 4 screws 270 and 3 screws 268.
- 3) Service Position can be achieved by flipping the analog board to the Vertical Position as shown in Figure 4-9.

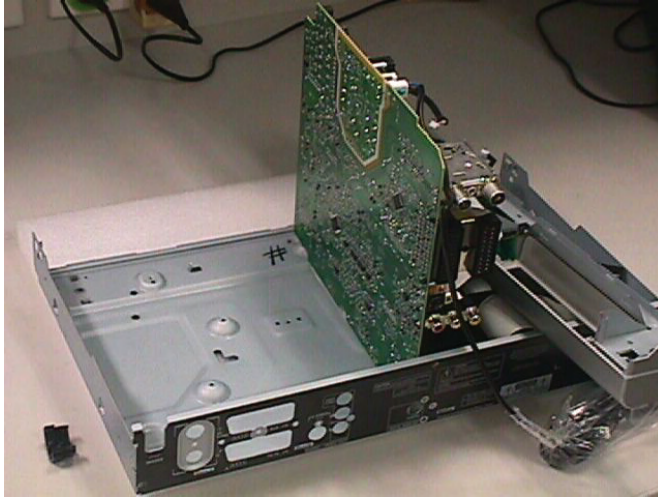


Figure 4-9

Note: Please cover the Live Area during trouble-shooting.
(Figure 4-10)

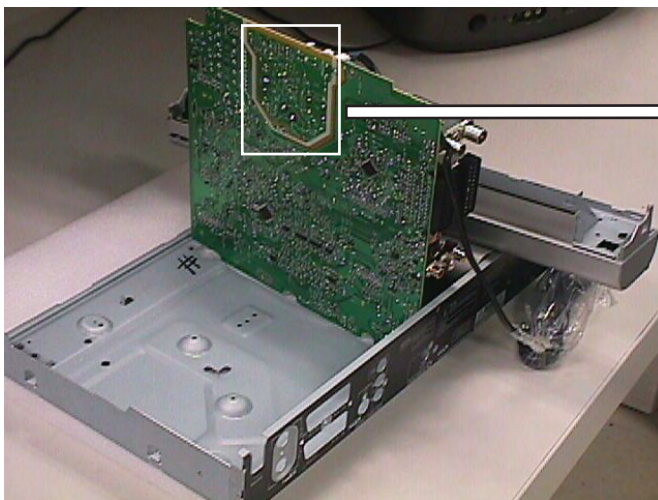


Figure 4-10

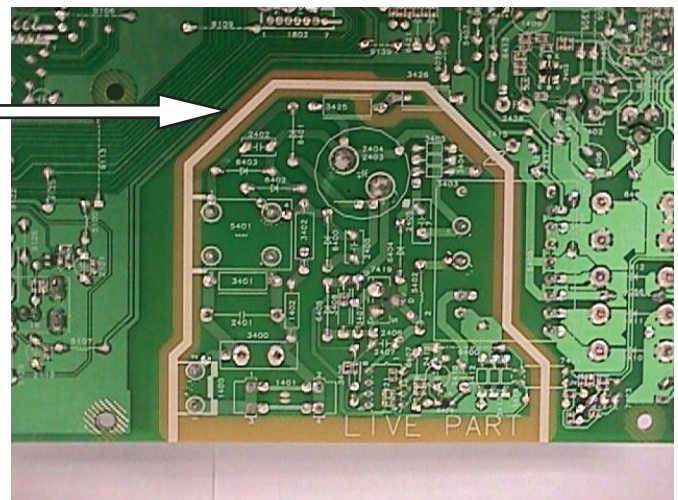


Figure Live Area

5. Upgrade Software & Repair Chart

5.1 Upgrade Software

A. Preparation to upgrade firmware:

1. Unzip the zip-archive file
2. Start the CD Burning software and create a new CD project (data disc) with the following settings:

File system	: Joliet
Format	: MODE 1: CDROM
Recording mode	: SINGLE SESSION (TRACK-AT-ONCE), FINALIZED CD

Note: Long file name is necessary for the preparation of the upgrade disc

3. Place the content of the zip-archive into the root directory of the new CD project.
4. Burn the data onto a blank CDR or CD-RW

B. Procedure to apply the firmware upgrade:

1. Power up the set and open tray.
2. Insert the prepared Upgrade CDROM and close the tray.
3. The TV connected to the set will display:

Software Upgrade Disc detected
Select OK to start or CANCEL to exit

4. Select OK or CANCEL with the <Right> or <Left> button and press <OK> button to confirm.
5. The TV connected to the set will display:

Upgrading Software, Please wait
Do not switch off the power

6. When the upgrading process is successful the tray will open and the TV connected to the set will display:

System is successfully upgraded.
Remove disc from tray & reset system

7. Remove the Upgrade Disc and press <OK> button on Remote control to confirm
8. The TV screen goes blank and the Philips Logo screen appear again after the tray door has closed.

C. How to Restore Factory setting (Default setting)

1. Power up the set and with no disc in the tray
2. Press <System Menu> <Right> and 4x <Down> buttons on the Remote control to reach the Restore Factory setting option.
3. Press <OK> button and the TV connected to the set will display:

System will reset to the Factory settings.
Select OK to confirm or CANCEL to exit.

4. Select OK or CANCEL with the <Right> or <Left> button and press <OK> button to confirm.

Note: All customers' settings will be lost.

D. How to read out the firmware version to confirm set has been upgraded.

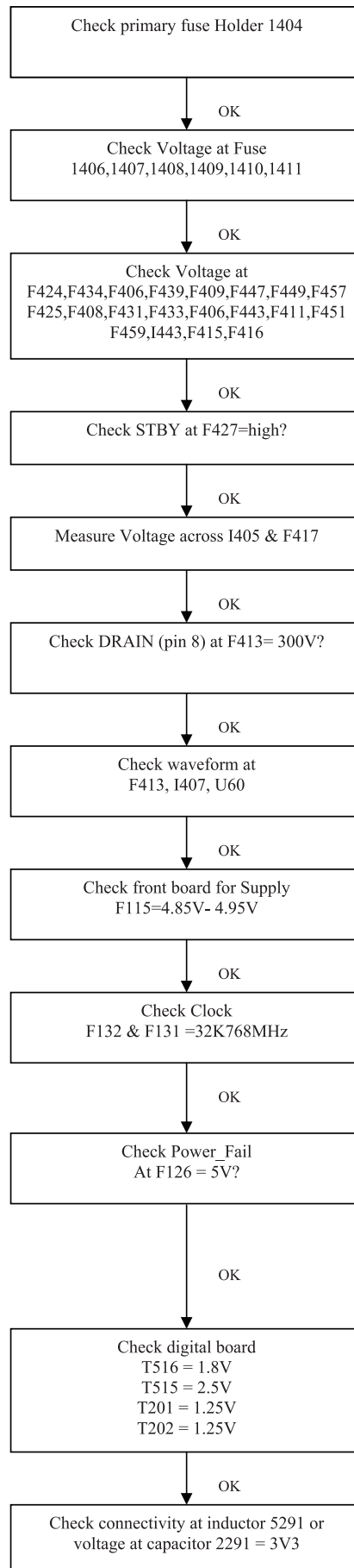
1. Power up the set and with no disc in the tray
2. Press <0009> and <OK> buttons on the Remote control
3. The TV connected to the set will display:

DVDR3365_75_BT3_2, Drive: 43.02.11 Build:
FAE6206 Apr 21 2005, 18:49:43

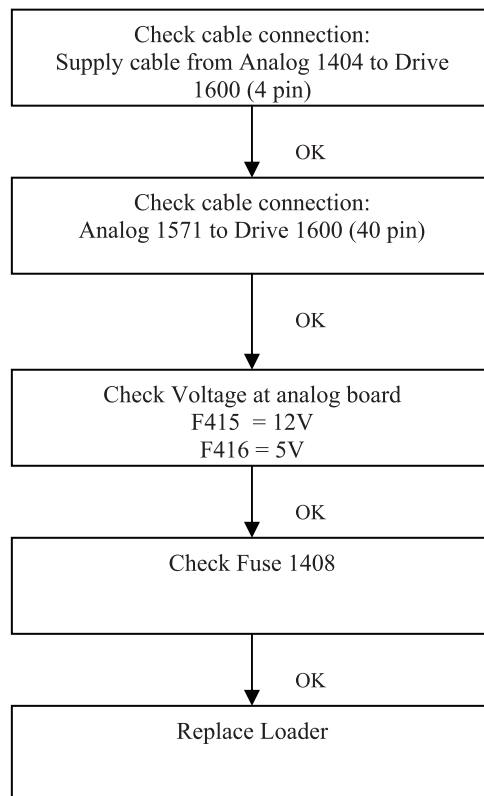
where DVDR3365_75 = Type/version
BT3_2 = Application (Backend) firmware version
43.02.11 = Drive (Basic Engine) firmware version

5.2 Repair Chart

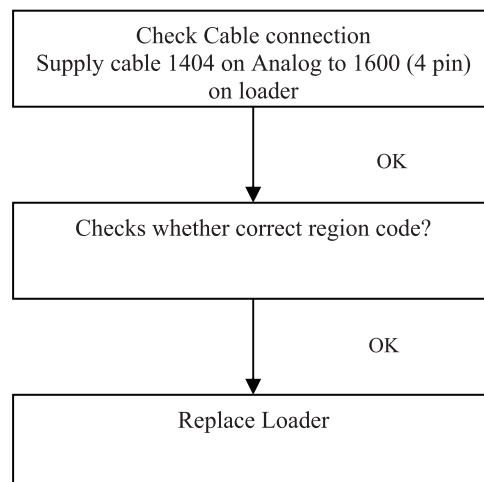
5.2.1 Completely Dead Set

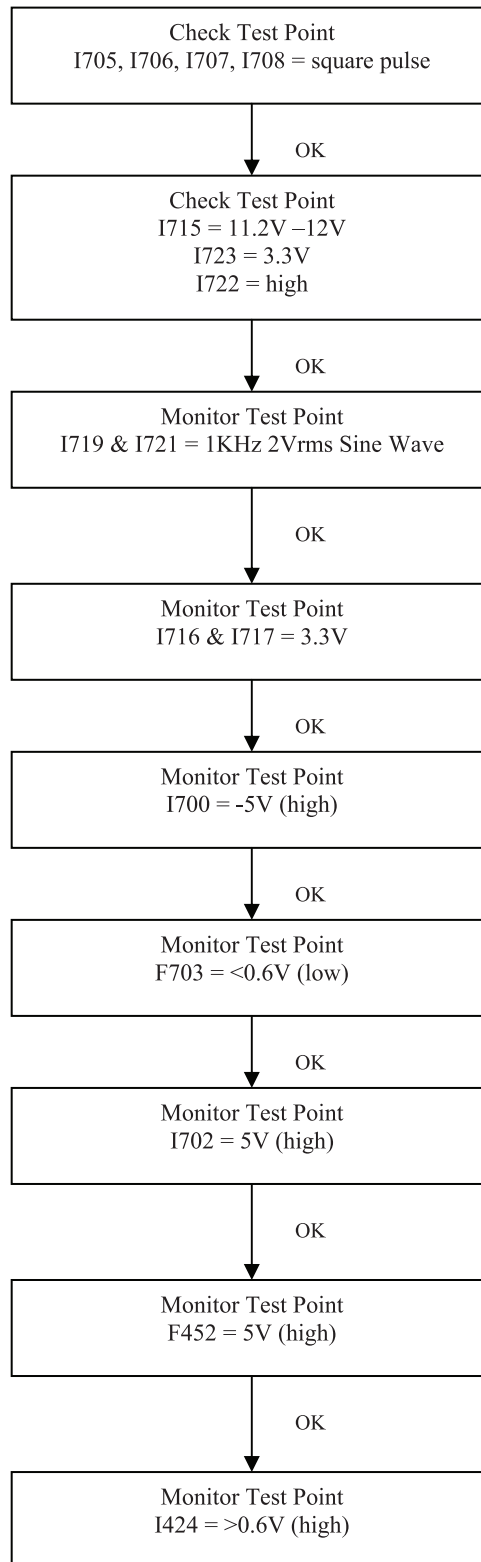


5.2.2 Cannot Read Disk



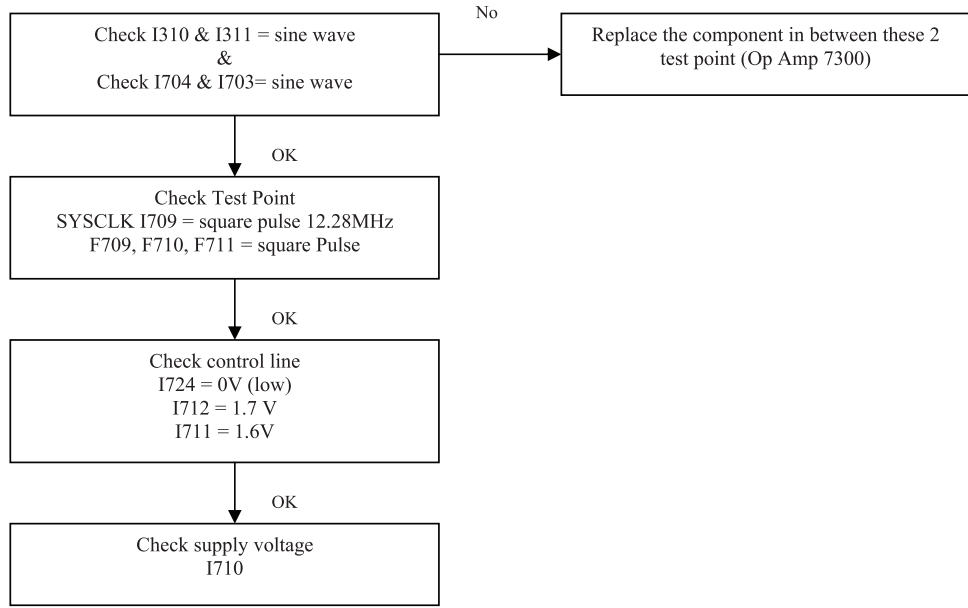
5.2.3 Disk Unknown



5.2.4 Audio No Sound (Playback)

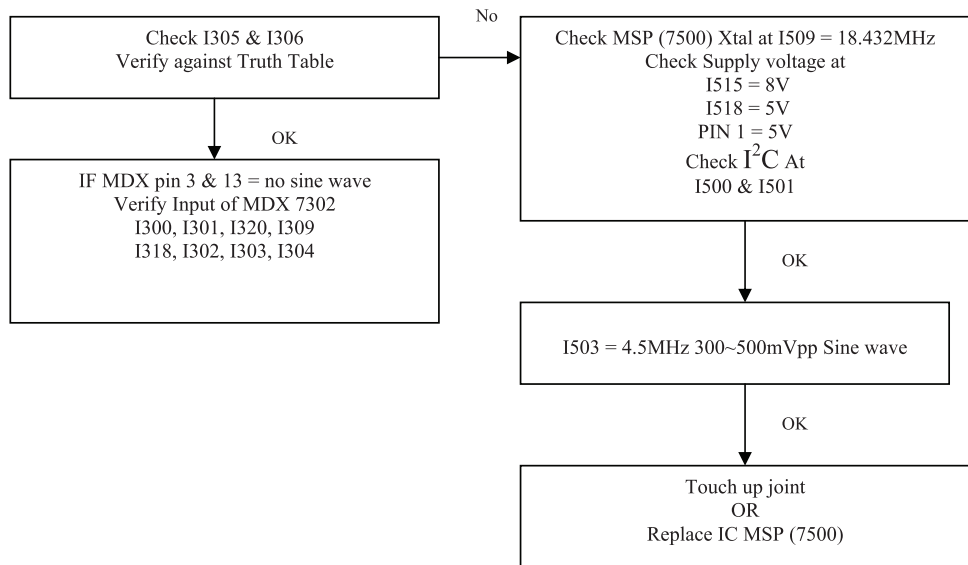
5.2.5 Audio No Sound (TV & External Source)

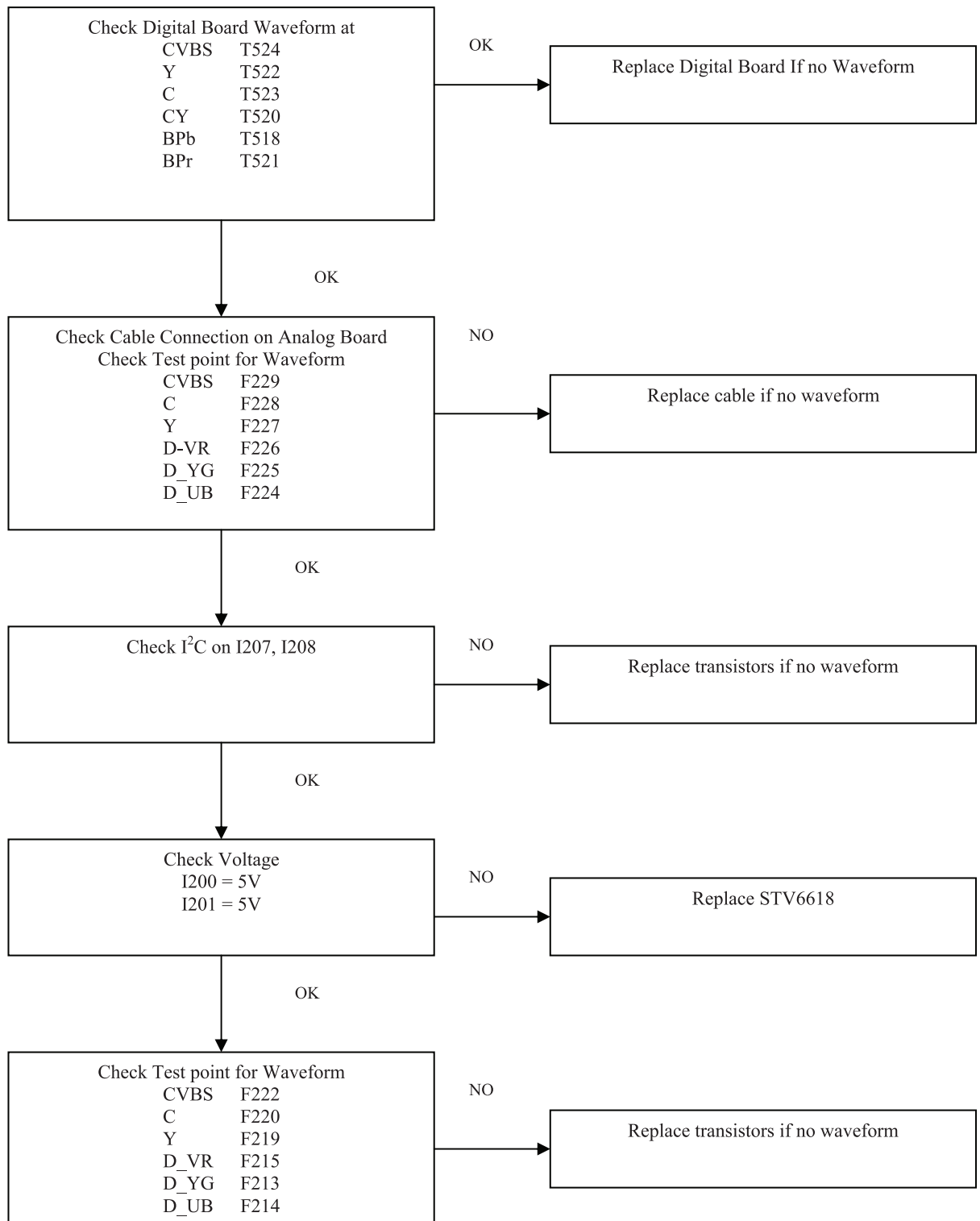
Part 1



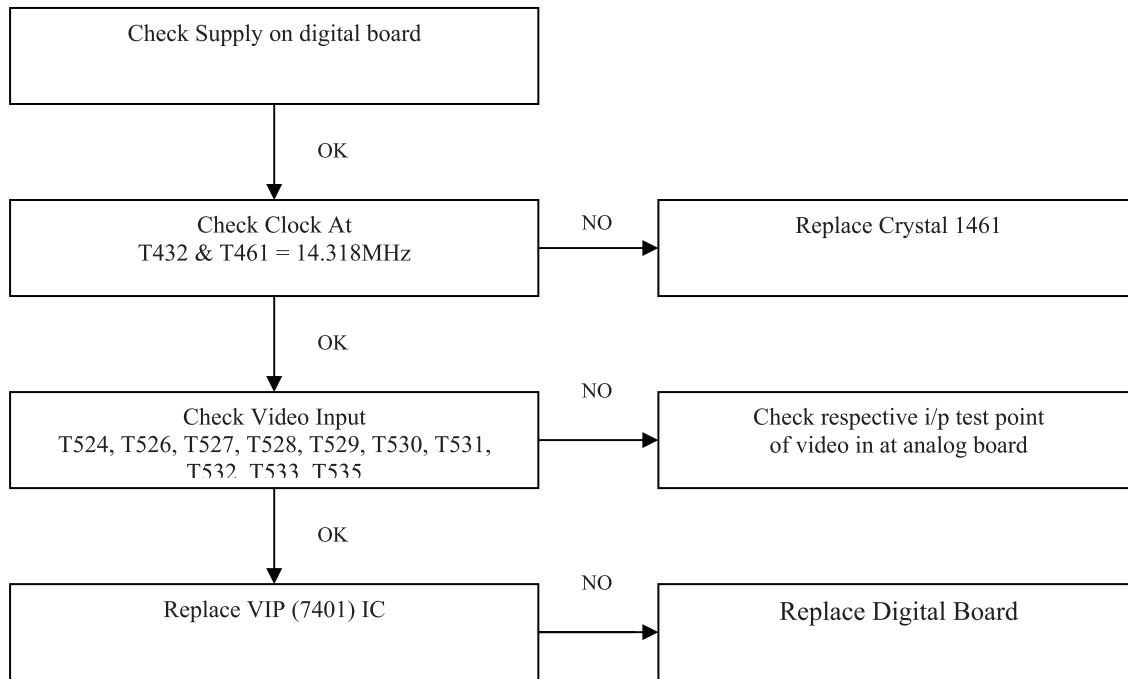
Part 2

Truth Table		
Pin 9	Pin 10	Source
0	0	Tuner
0	1	SCART 2
1	0	SCART 1
1	1	FRONT AV IN

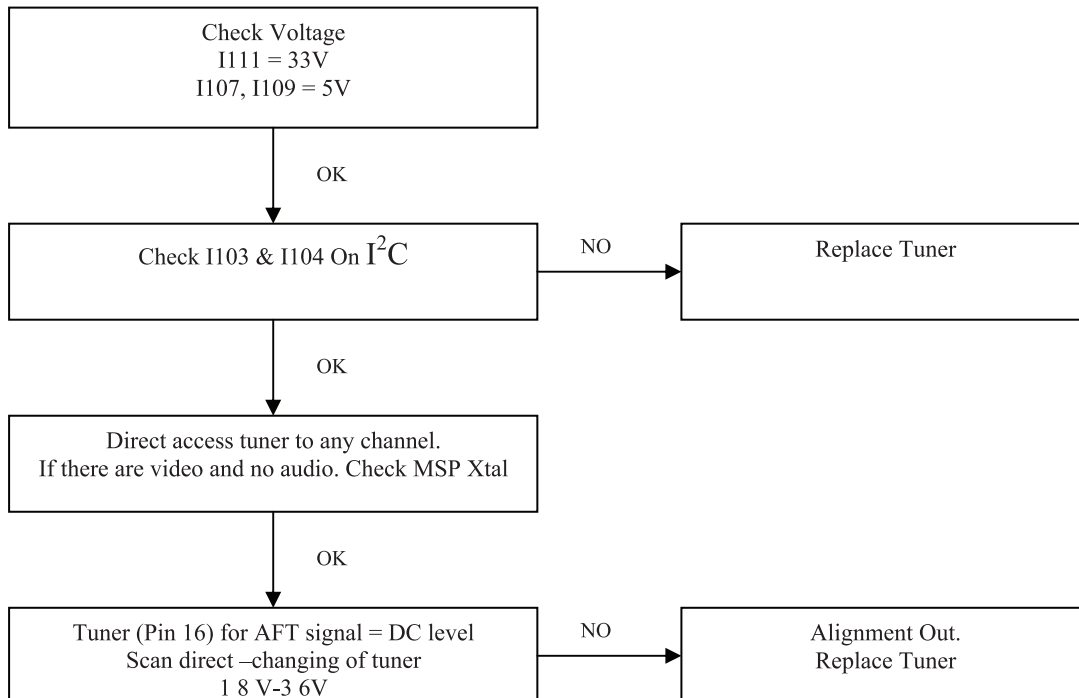


5.2.6 No Video Out Upon Power ON (Assume set is not dead)

5.2.7 No Video In Only

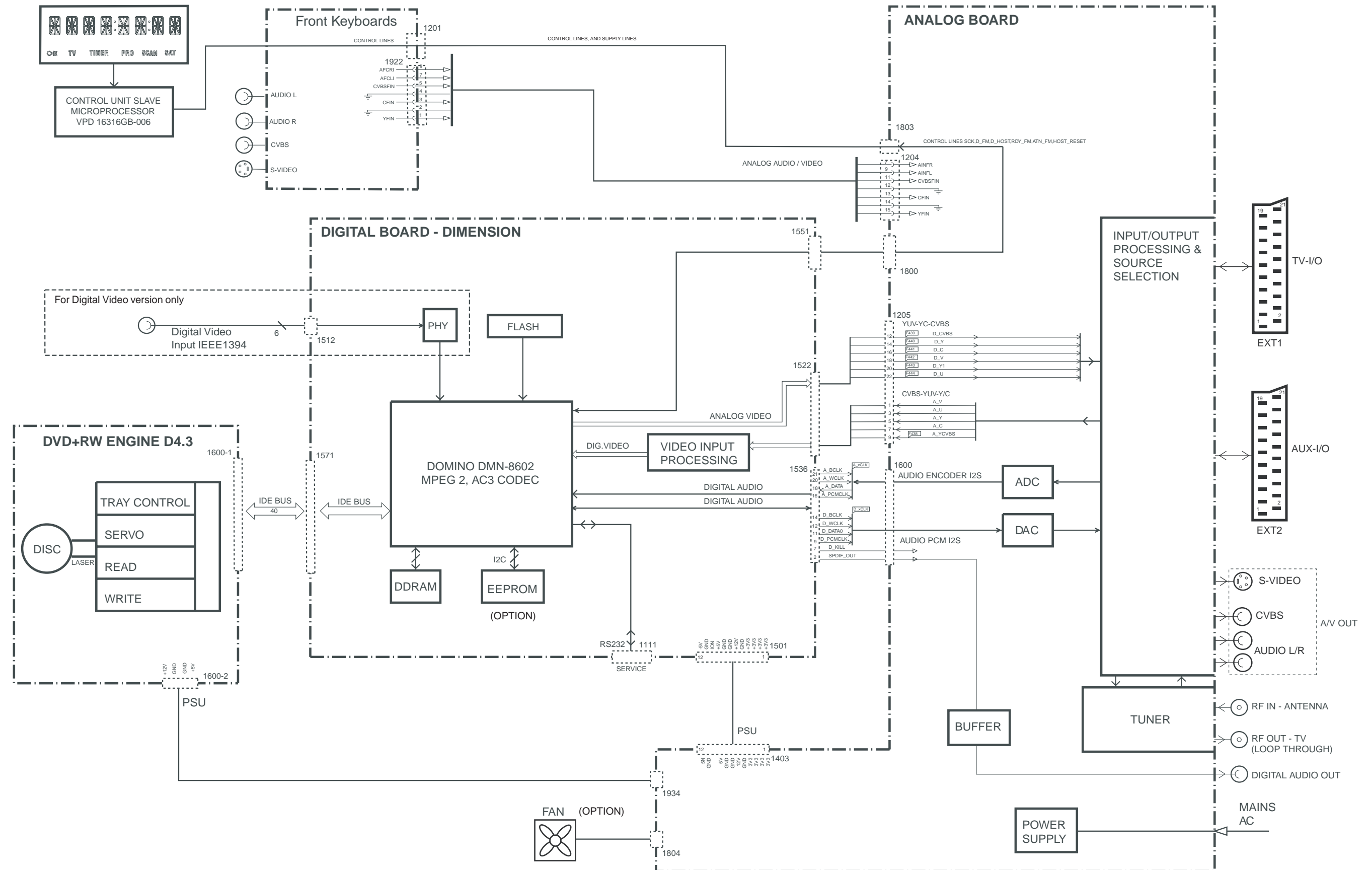


5.2.8 Tuner Not Functioning

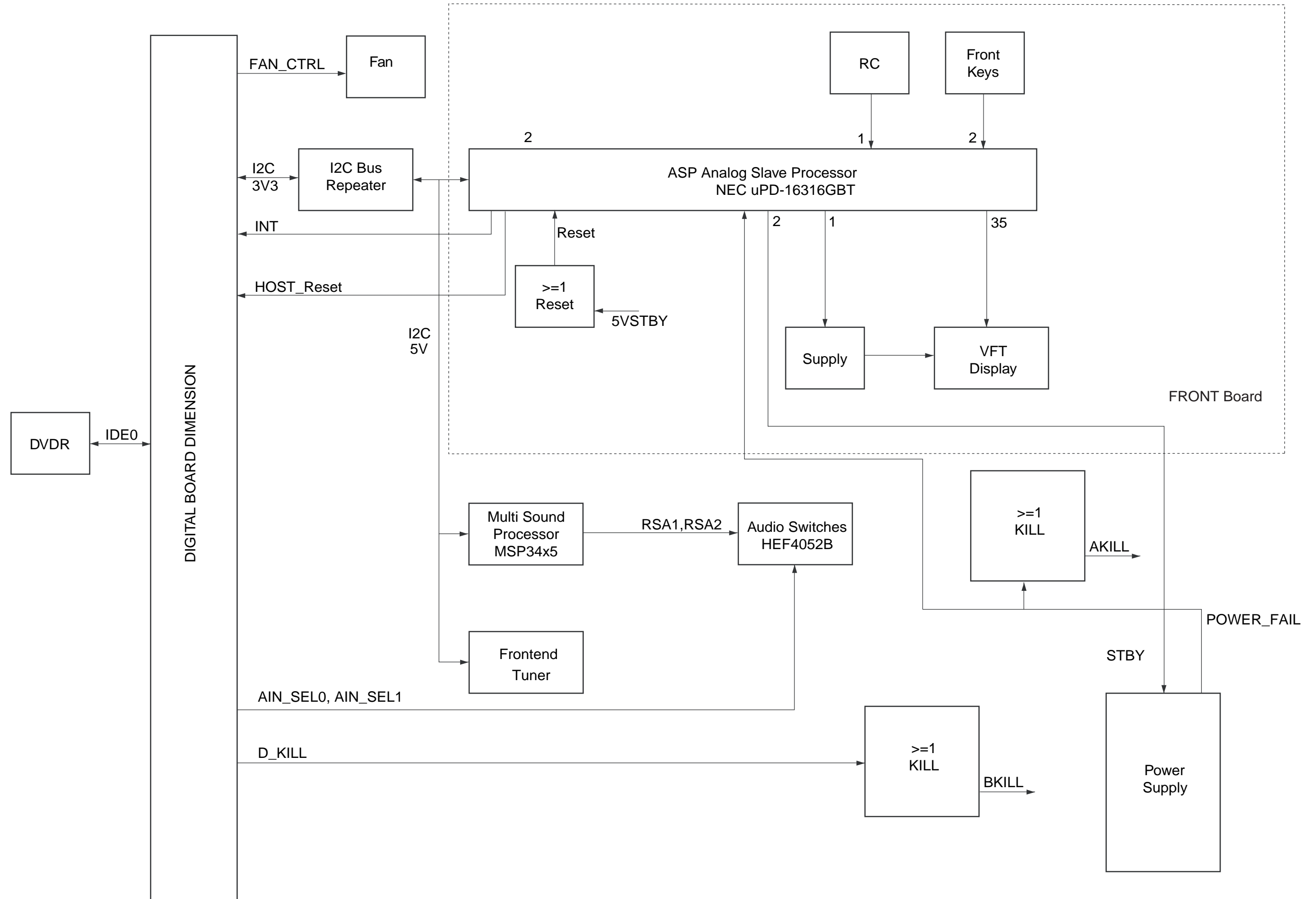


6. Block Diagrams, Waveforms, Wiring Diagram

Overall Block Diagram of the Set

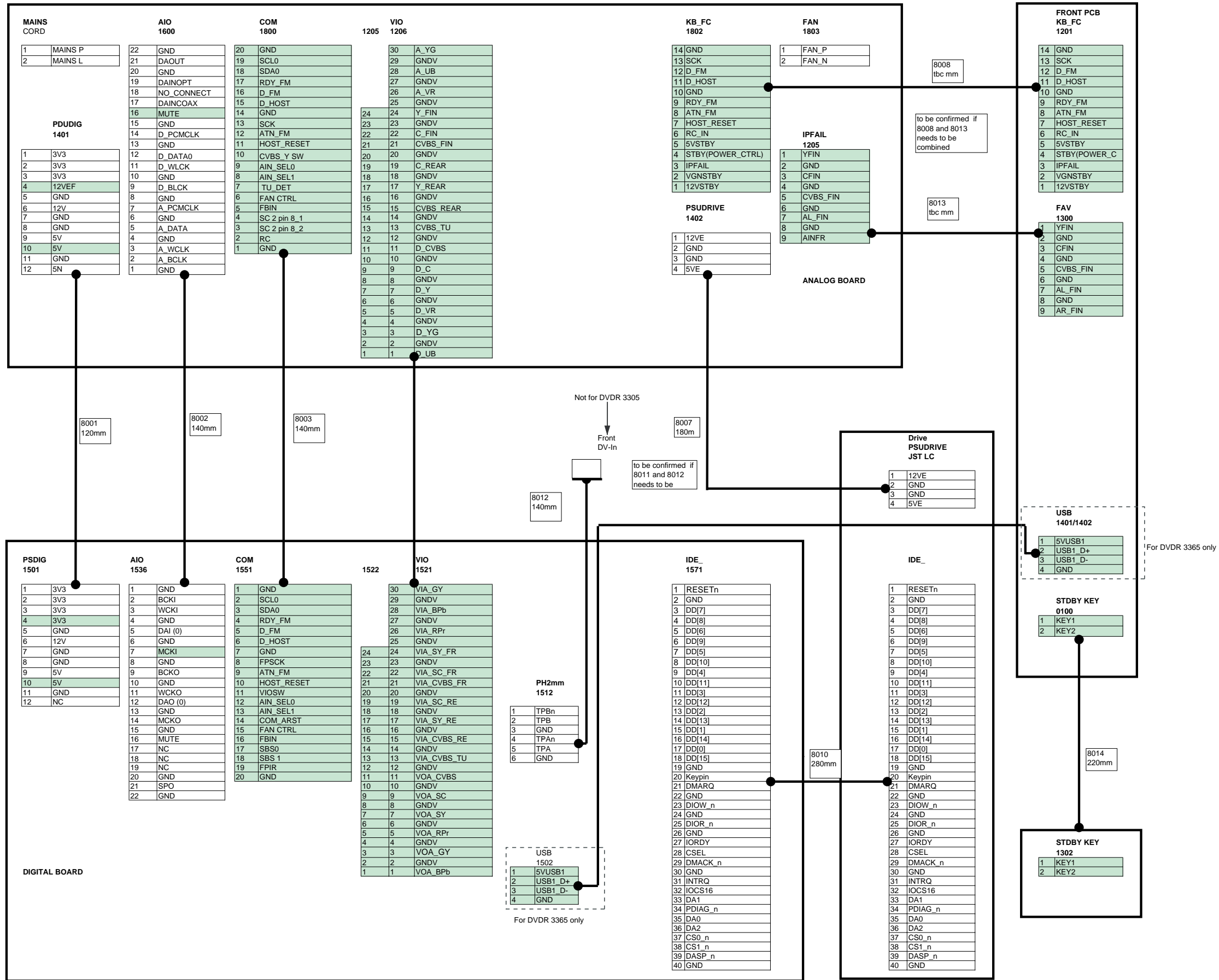


Control Block Diagram
Control Block Diagram Analog Board



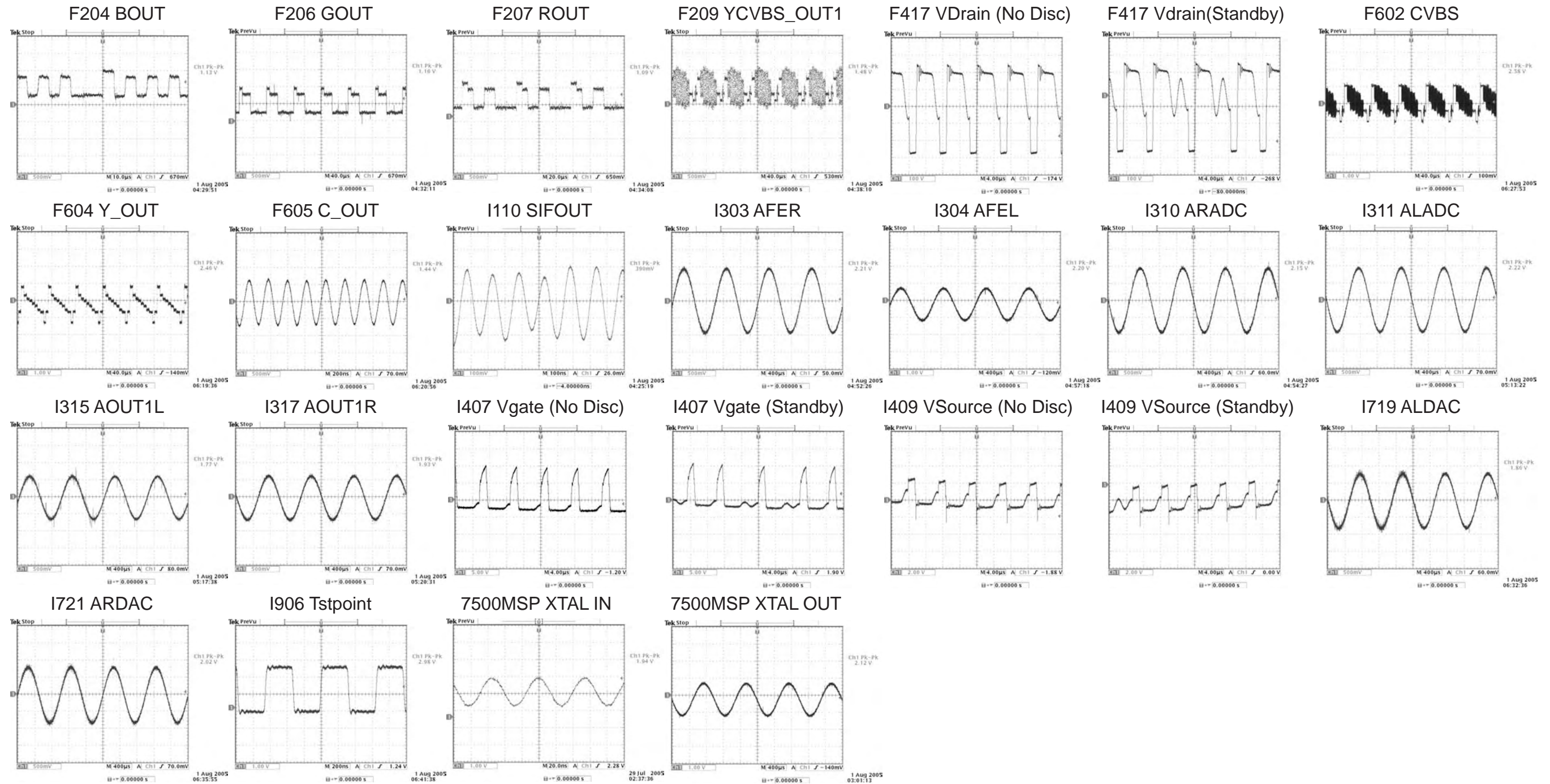
Wiring Diagram

Interconnection Diagram Architecture

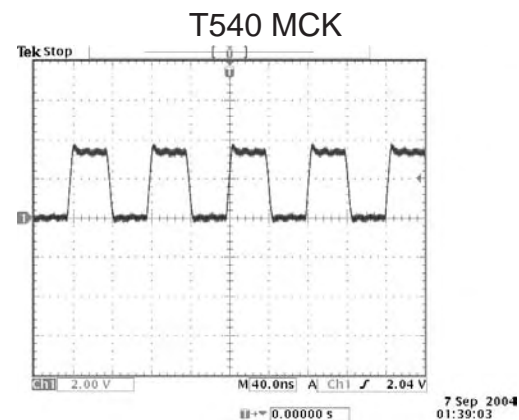
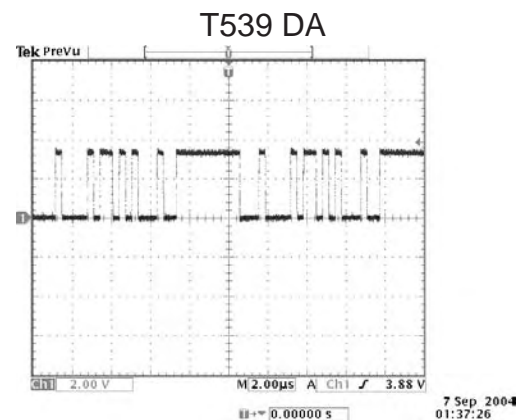
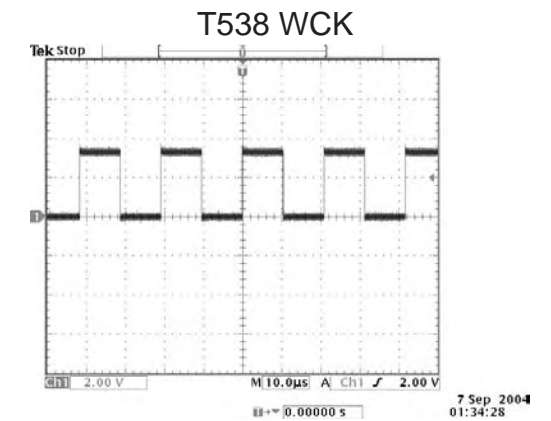
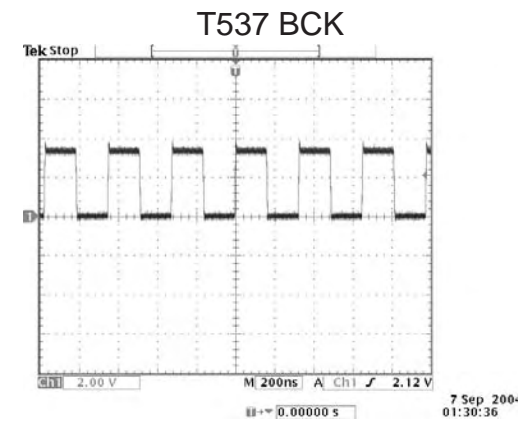
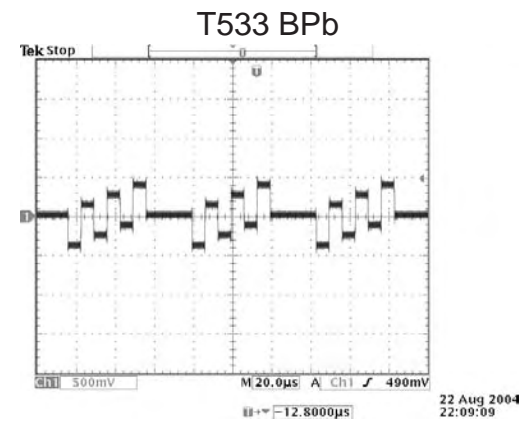
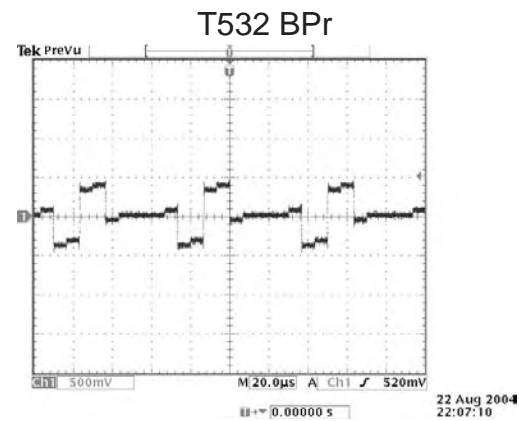
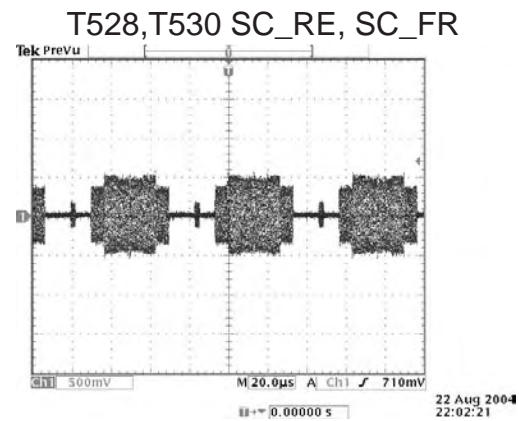
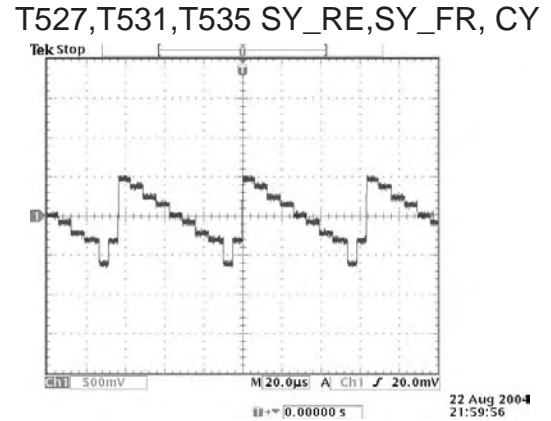
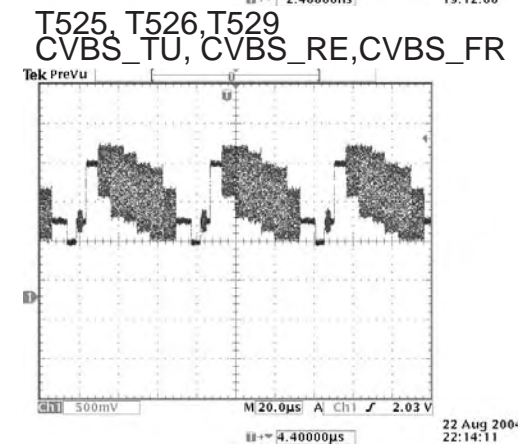
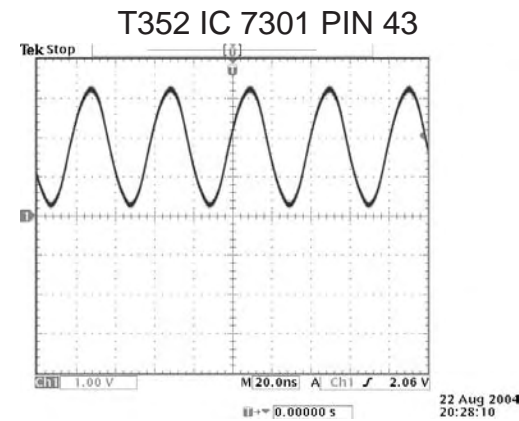
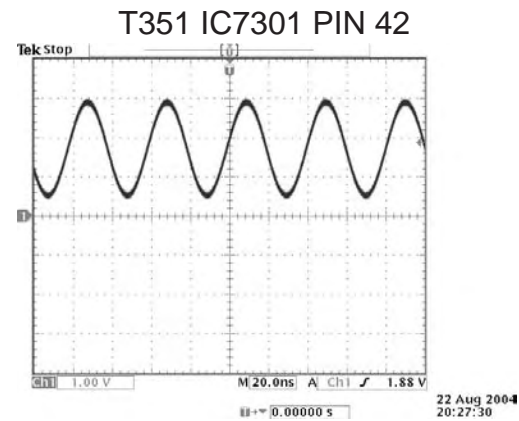
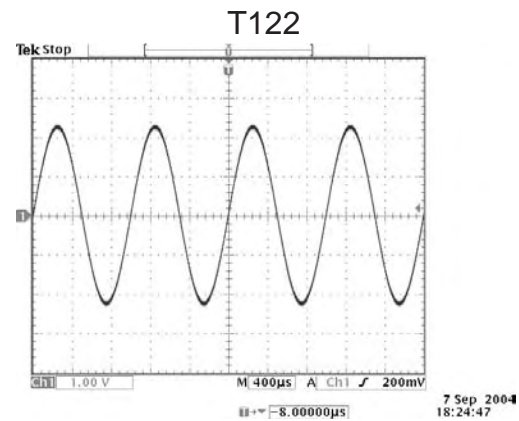
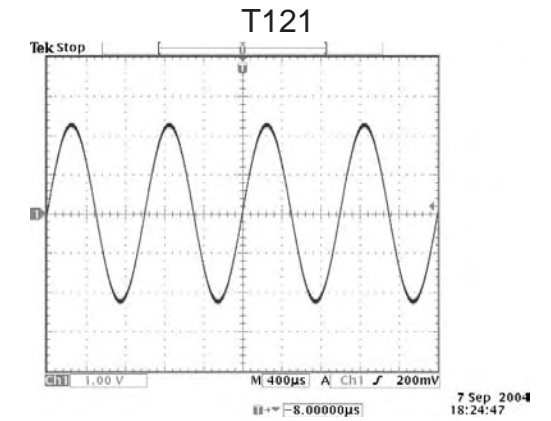
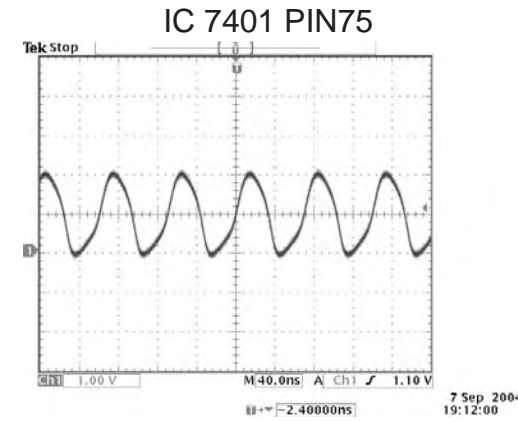
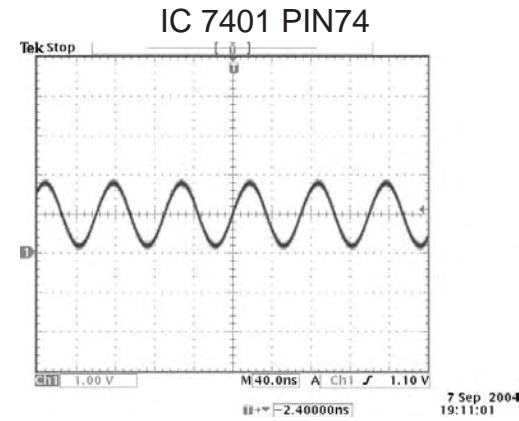
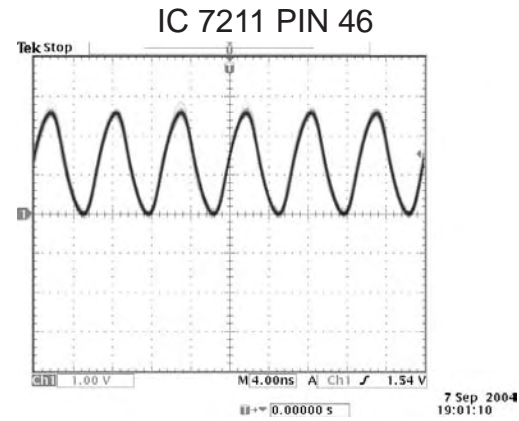
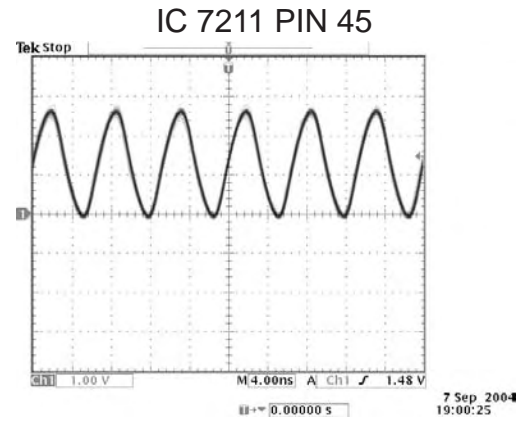


Waveforms

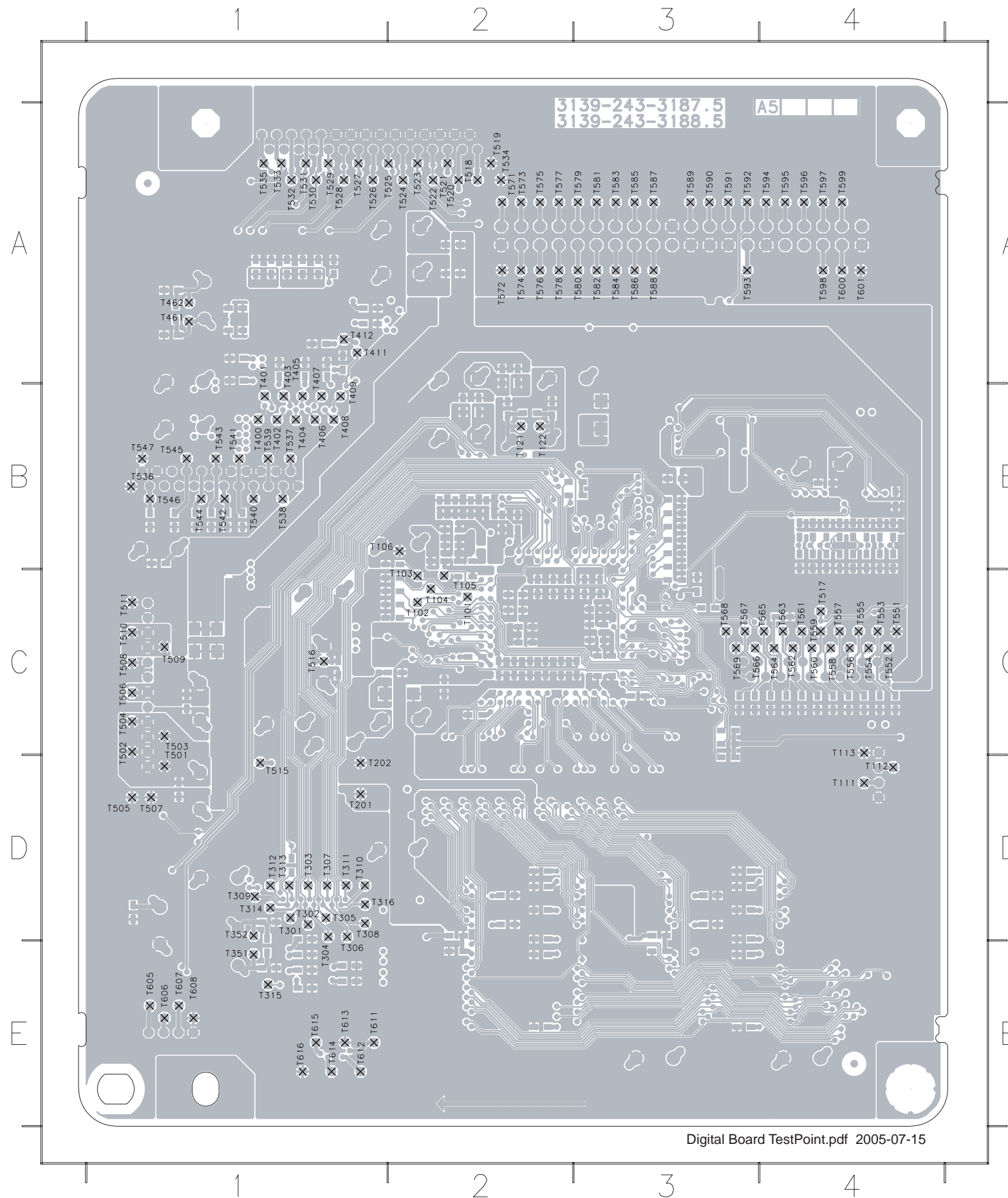
Waveforms of Analog Board



Waveforms of Digital Board



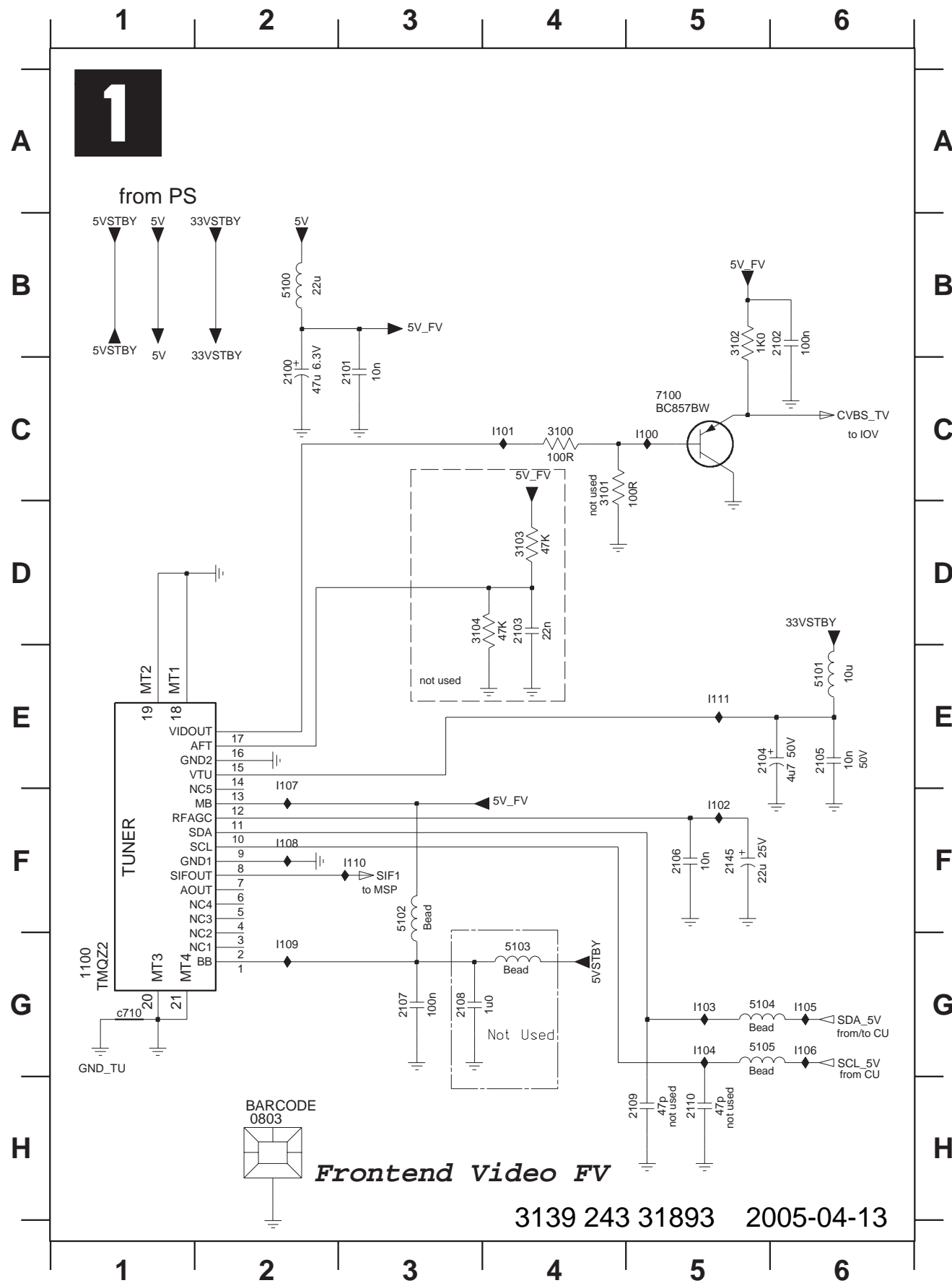
Test Points Overview for Digital Board



T101	C2
T102	C2
T103	C2
T104	C2
T105	C2
T106	B2
T111	D4
T112	D4
T113	C4
T121	B2
T122	B2
T201	D1
T202	D1
T301	D1
T302	D1
T303	D1
T304	D1
T305	D1
T306	D1
T307	D1
T310	D1
T311	D1
T312	D1
T313	D1
T314	D1
T315	F1
T316	F1
T351	F1
T352	F1
T400	B1
T401	B1
T402	B1
T403	B1
T404	B1
T405	B1
T406	B1
T407	B1
T408	B1
T409	B1
T411	A1
T412	A1
T461	A1
T501	D1
T502	D1
T503	C1
T504	C1
T505	D1
T506	C1
T507	D1
T508	C1
T509	C1
T510	C1
T511	C1
T515	C1
T516	C1
T517	C1
T518	C4
T519	C4
T520	A2
T521	A2
T522	A2
T523	A2
T524	A2
T525	A1
T526	A1
T527	A1
T528	A1
T529	A1
T530	A1
T531	A1
T532	A1
T533	A1
T534	A2
T535	A1
T536	B1
T537	B1
T538	B1
T539	B1
T540	B1
T541	B1
T542	B1
T543	B1
T544	B1
T545	B1
T546	B1
T547	B1
T548	B1
T549	B1
T550	B1
T551	B1
T552	B1
T553	B1
T554	B1
T555	B1
T556	B1
T557	B1
T558	B1
T559	B1
T560	B1
T561	B1
T562	B1
T563	B1
T564	B1
T565	B1
T566	B1
T567	B1
T568	B1
T569	B1
T570	B1
T571	B1
T572	B1
T573	B1
T574	B1
T575	B1
T576	B1
T577	B1
T578	B1
T579	B1
T580	B1
T581	B1
T582	B1
T583	B1
T584	B1
T585	B1
T586	B1
T587	B1
T588	B1
T589	B1
T590	B1
T591	B1
T592	B1
T593	B1
T594	B1
T595	B1
T596	B1
T597	B1
T598	B1
T599	B1
T600	B1
T601	B1
T602	B1
T603	B1
T604	B1
T605	B1
T606	B1
T607	B1
T608	B1
T609	B1
T610	B1
T611	B1
T612	B1
T613	B1
T614	B1
T615	B1
T616	B1
T617	B1
T618	B1
T619	B1
T620	B1
T621	B1
T622	B1
T623	B1
T624	B1
T625	B1
T626	B1
T627	B1
T628	B1
T629	B1
T630	B1
T631	B1
T632	B1
T633	B1
T634	A2
T635	A1
T636	B1
T637	B1
T638	B1
T639	B1
T640	B1
T641	B1
T642	B1
T643	B1
T644	B1

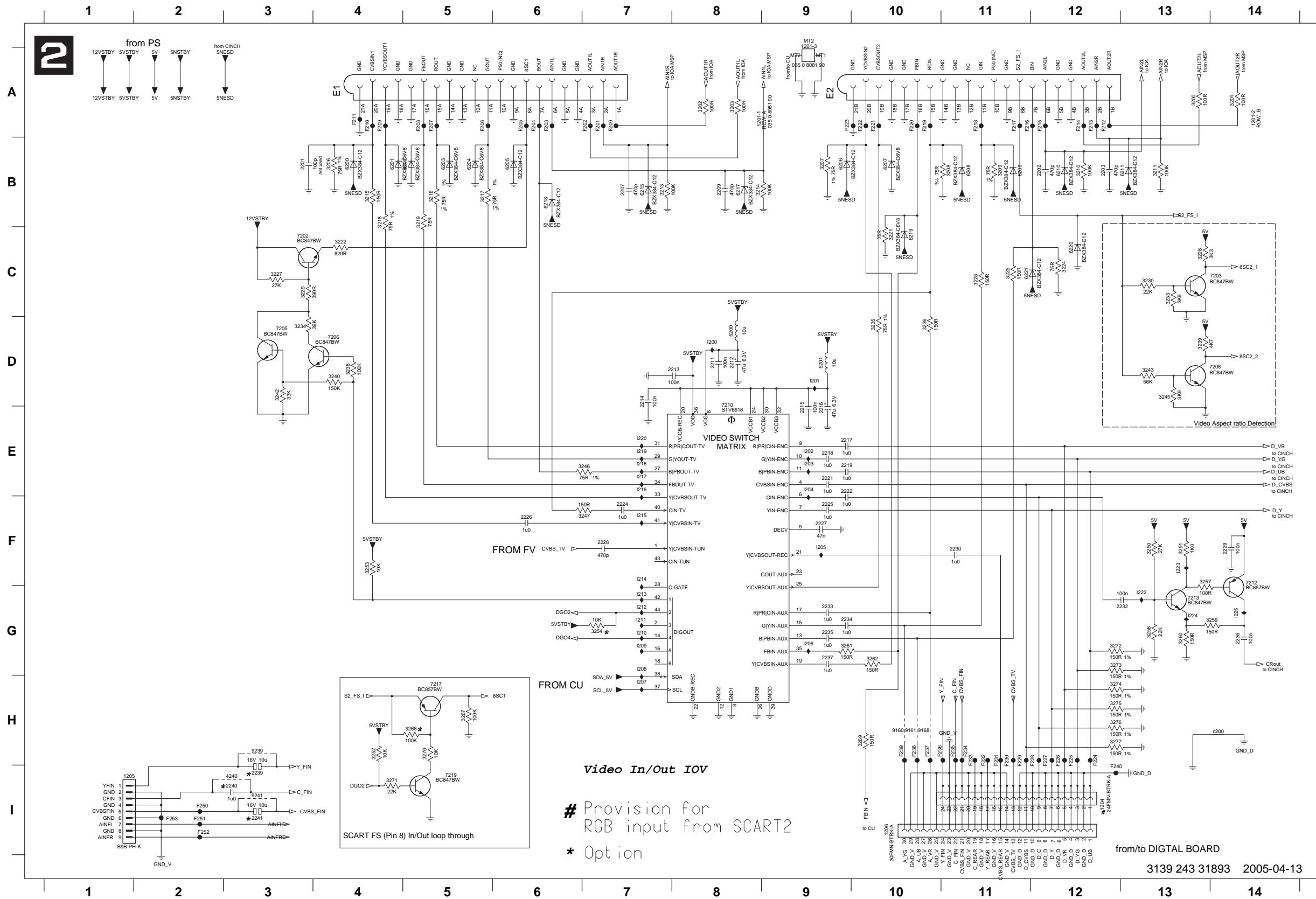
7. Circuit Diagrams and PWB Layouts

Analog: Frontend Video (FV)



- 0803 H2
- 1100 G1
- 2100 C2
- 2101 C3
- 2102 B6
- 2103 D4
- 2104 E5
- 2105 E6
- 2106 F5
- 2107 G3
- 2108 G3
- 2109 H5
- 2110 H5
- 2145 F5
- 3100 C4
- 3101 C4
- 3102 B5
- 3103 D4
- 3104 D3
- 5100 B2
- 5101 E6
- 5102 F3
- 5103 G4
- 5104 G5
- 5105 G5
- 7100 C5
- I100 C5
- I101 C4
- I102 F5
- I103 G5
- I104 G5
- I105 G6
- I106 G6
- I107 E2
- I108 F2
- I109 G2
- I110 F3
- I111 E5
- c710 G1

Analog: Video In / Out (IOV)



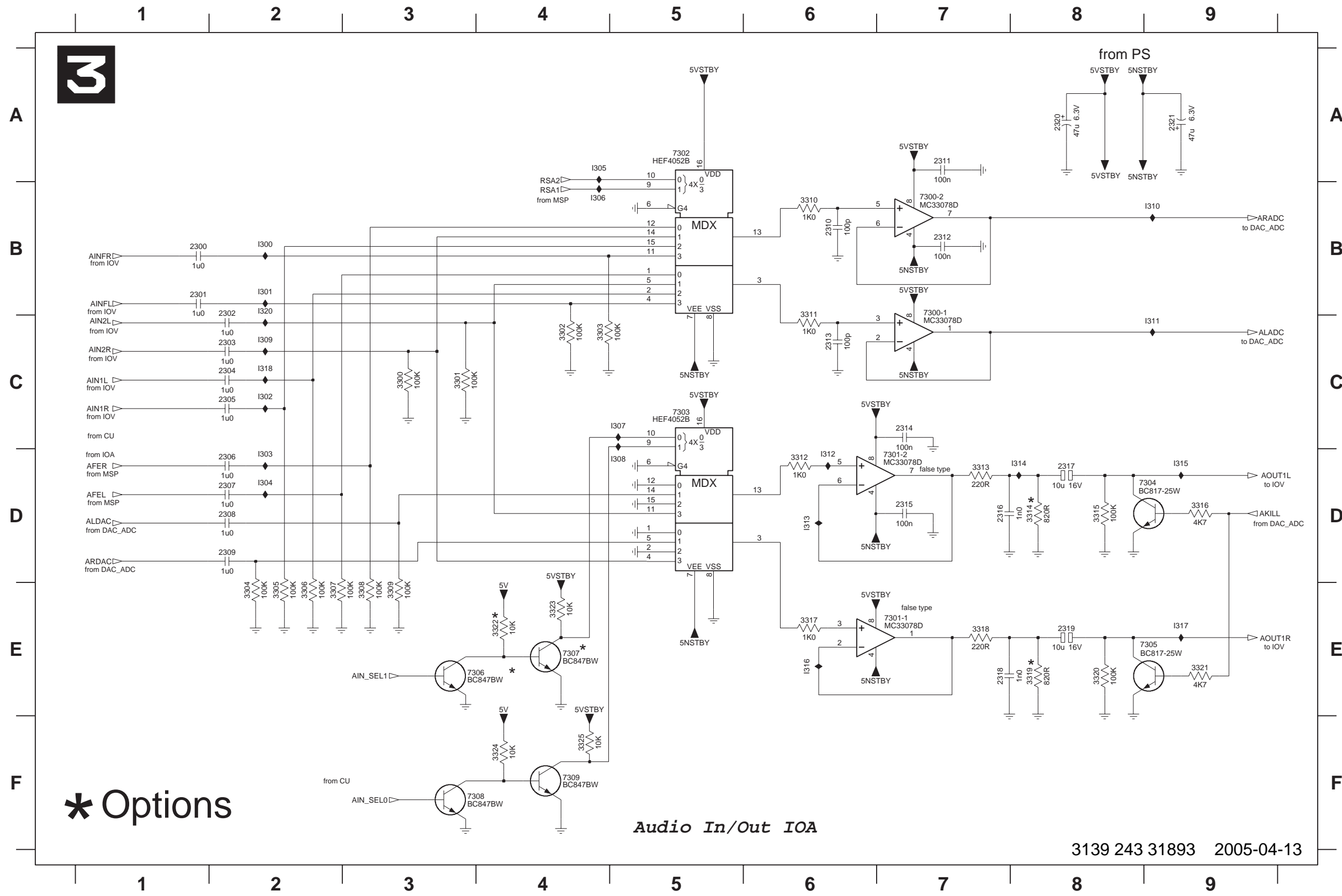
- 1201-1 A8
- 1201-2 A14
- 1201-3 A9
- 1204 H2
- 1205 H
- 1206 H10
- 1201 B3
- 2202 B12
- 2203 B12
- 2207 B7
- 2209 B6
- 2211 D8
- 2212 D8
- 2213 D8
- 2214 D7
- 2215 E9
- 2216 E9
- 2217 E9
- 2218 E9
- 2219 E9
- 2221 E9
- 2222 E9
- 2224 F7
- 2225 F9
- 2226 F6
- 2227 F9
- 2228 F7
- 2229 F14
- 2230 F11
- 2232 G13
- 2233 G9
- 2234 G9
- 2235 G9
- 2236 G14
- 2237 G9
- 2239 I3
- 2240 I3
- 2241 I3
- 3200 A13
- 3201 A14
- 3202 A8
- 3203 A8
- 3206 B4
- 3207 B9
- 3208 B11
- 3209 B11
- 3210 B12
- 3211 B13
- 3213 B7
- 3214 B8
- 3215 B4
- 3216 B5
- 3217 B5
- 3218 B4
- 3219 B5
- 3221 C10
- 3222 C4
- 3224 C12
- 3225 C11
- 3226 C13
- 3227 C3
- 3228 C11
- 3229 C3
- 3230 C13
- 3233 C13
- 3234 D3
- 3235 D10
- 3236 D10
- 3238 D4
- 3239 D13
- 3240 D4
- 3242 D3
- 3243 D13
- 3245 D13
- 3246 E7
- 3247 F7
- 3250 F13
- 3251 F13
- 3252 H4
- 3253 F4
- 3254 G7
- 3257 F13
- 3258 G13
- 3259 G14
- 3260 G13
- 3261 G9
- 3262 G10
- 3267 H5
- 3268 H5
- 3269 H10
- 3270 H5
- 3271 I4
- 3272 G12
- 3273 G12
- 3274 H12
- 3275 H12
- 3276 H12
- 3277 H12
- 4240 I3
- 5200 D8
- 5201 D9
- 6200 B4
- 6201 B4
- 6202 B5
- 6203 B5
- 6204 B5
- 6205 B6
- 6206 B9
- 6207 B10
- 6208 B11
- 6209 B11
- 6210 B12
- 6211 B13
- 6215 B7
- 6217 B8
- 6218 B6
- 6219 C10
- 6220 C12
- 6221 C11
- 7202 C3
- 7203 C14
- 7205 D3
- 7206 D4
- 7208 D14
- 7210 E8
- 7212 F14
- 7213 G13
- 7217 H5
- 7219 I5
- 9169 H10
- 9161 H10
- 9168 H10
- 9239 H3
- 9241 I3
- F209 A7
- F201 A7
- F202 A7
- F203 A6
- F204 A6
- F205 A6
- F206 A5
- F207 A5
- F208 A5
- F209 A4
- F210 A4
- F211 A4
- F212 A2
- F213 A2
- F214 A2
- F215 A12
- F216 A11
- F217 A11
- F218 A10
- F219 A10
- F220 A10
- F221 A10
- F222 A10
- F223 A9
- F224 H12
- F225 H12
- F226 H12
- F227 H12
- F228 H12
- F229 H11
- F230 H11
- F231 H11
- F232 H11
- F233 H11
- F234 H11
- F235 H11
- F236 H11
- F237 H10
- F238 H10
- F239 H10
- F240 H12
- F250 I2
- F251 I2
- F252 I2
- F253 I2
- I200 D8
- I201 D9
- I202 E9
- I203 E9
- I205 F9
- I206 G9
- I207 H7
- I208 G7
- I209 G7
- I210 G7
- I211 G7
- I212 G7
- I213 G7
- I214 F7
- I215 F7
- I216 E7
- I217 E7
- I218 E7
- I219 E7
- I220 E7
- I222 G13
- I223 F13
- I224 G13
- I225 G14
- c200 H14

Video In/Out IOV

Provision for RGB input from SCART2

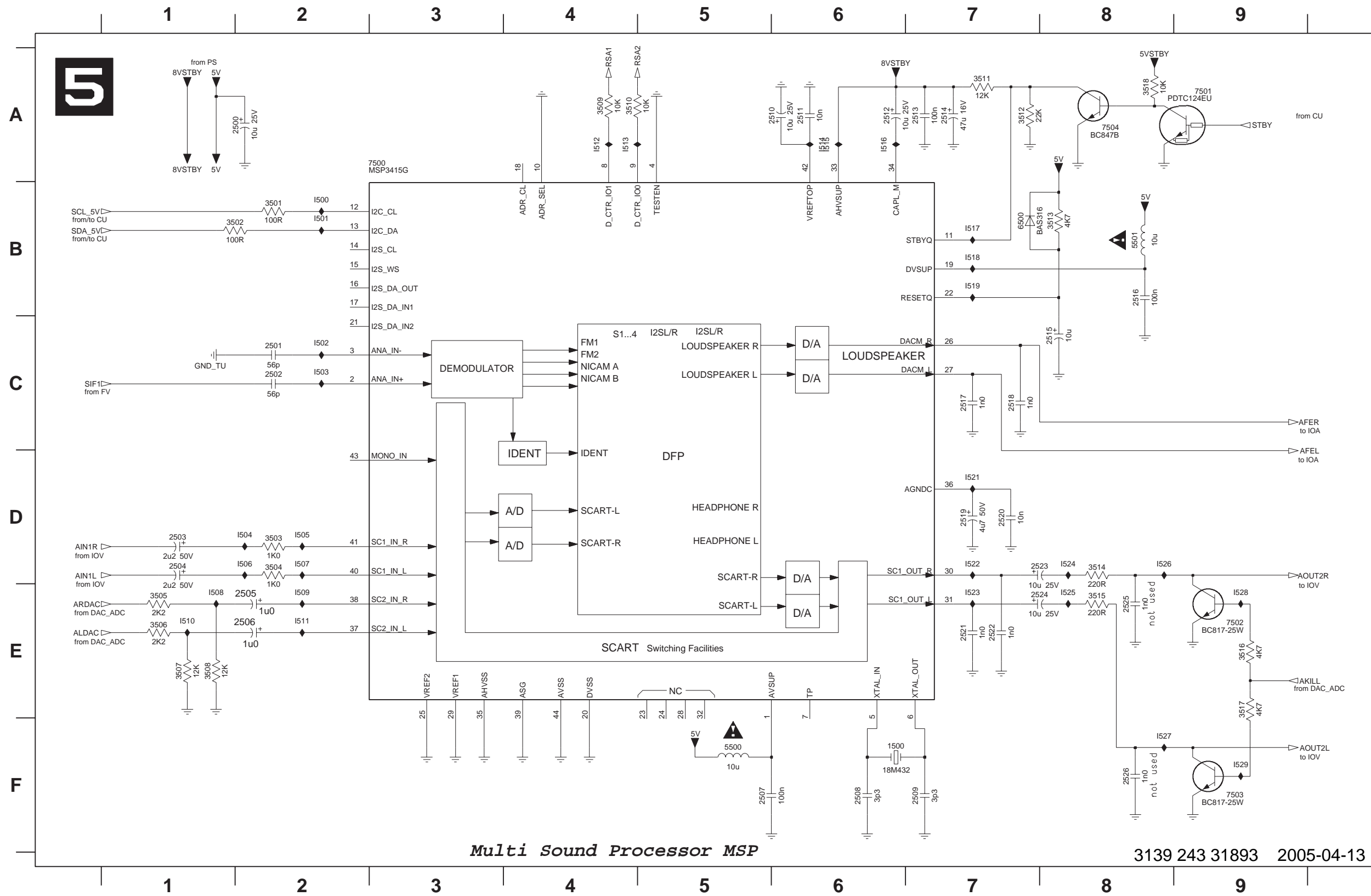
* Option

Analog: Audio In / Out (IOA)



- 2300 B1
- 2301 B1
- 2302 C2
- 2303 C2
- 2304 C2
- 2305 C2
- 2306 D2
- 2307 D2
- 2308 D2
- 2309 D2
- 2310 B6
- 2311 A7
- 2312 B7
- 2313 C6
- 2314 C7
- 2315 D7
- 2316 D7
- 2317 D8
- 2318 E7
- 2319 E8
- 2320 A8
- 2321 A9
- 3300 C3
- 3301 C3
- 3302 C4
- 3303 C4
- 3304 E2
- 3305 E2
- 3306 E2
- 3307 E2
- 3308 E3
- 3309 E3
- 3310 B6
- 3311 C6
- 3312 D6
- 3313 D7
- 3314 D8
- 3315 D8
- 3316 D9
- 3317 E6
- 3318 E7
- 3319 E8
- 3320 E8
- 3321 E9
- 3322 E4
- 3323 E4
- 3324 F4
- 3325 F4
- 7300-1 B7
- 7300-2 B7
- 7301-1 E7
- 7301-2 D7
- 7302 A5
- 7303 C5
- 7304 D9
- 7305 E9
- 7306 E3
- 7307 E4
- 7308 F3
- 7309 F4
- I300 B2
- I301 B2
- I302 C2
- I303 D2
- I304 D2
- I305 A4
- I306 B4
- I307 C5
- I308 D5
- I309 C2
- I310 B9
- I311 C9
- I312 D6
- I313 D6
- I314 D8
- I315 D9
- I316 E6
- I317 E9
- I318 C2
- I320 B2

Analog: Multi Sound Processing (MSP)

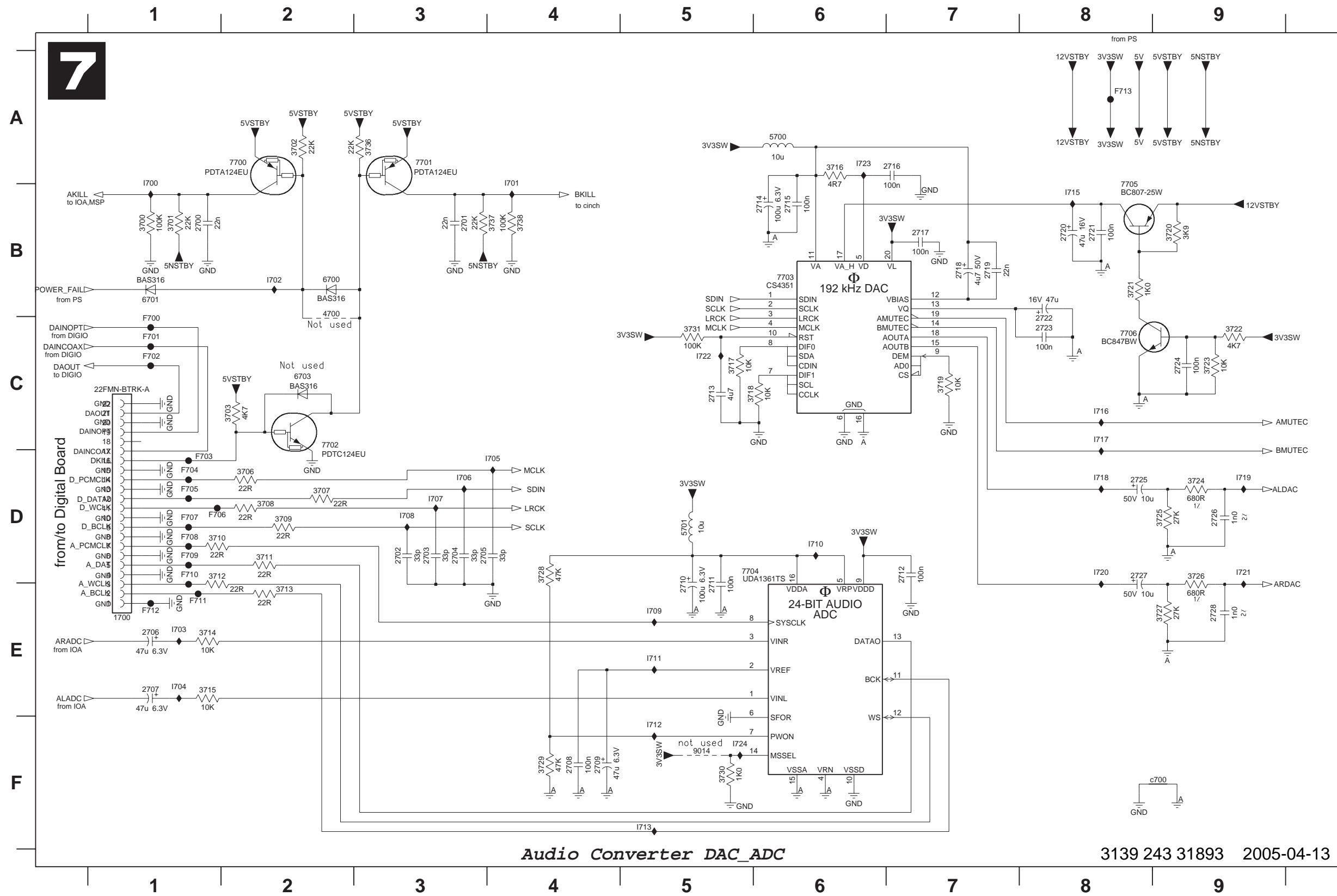


Multi Sound Processor MSP

3139 243 31893 2005-04-13

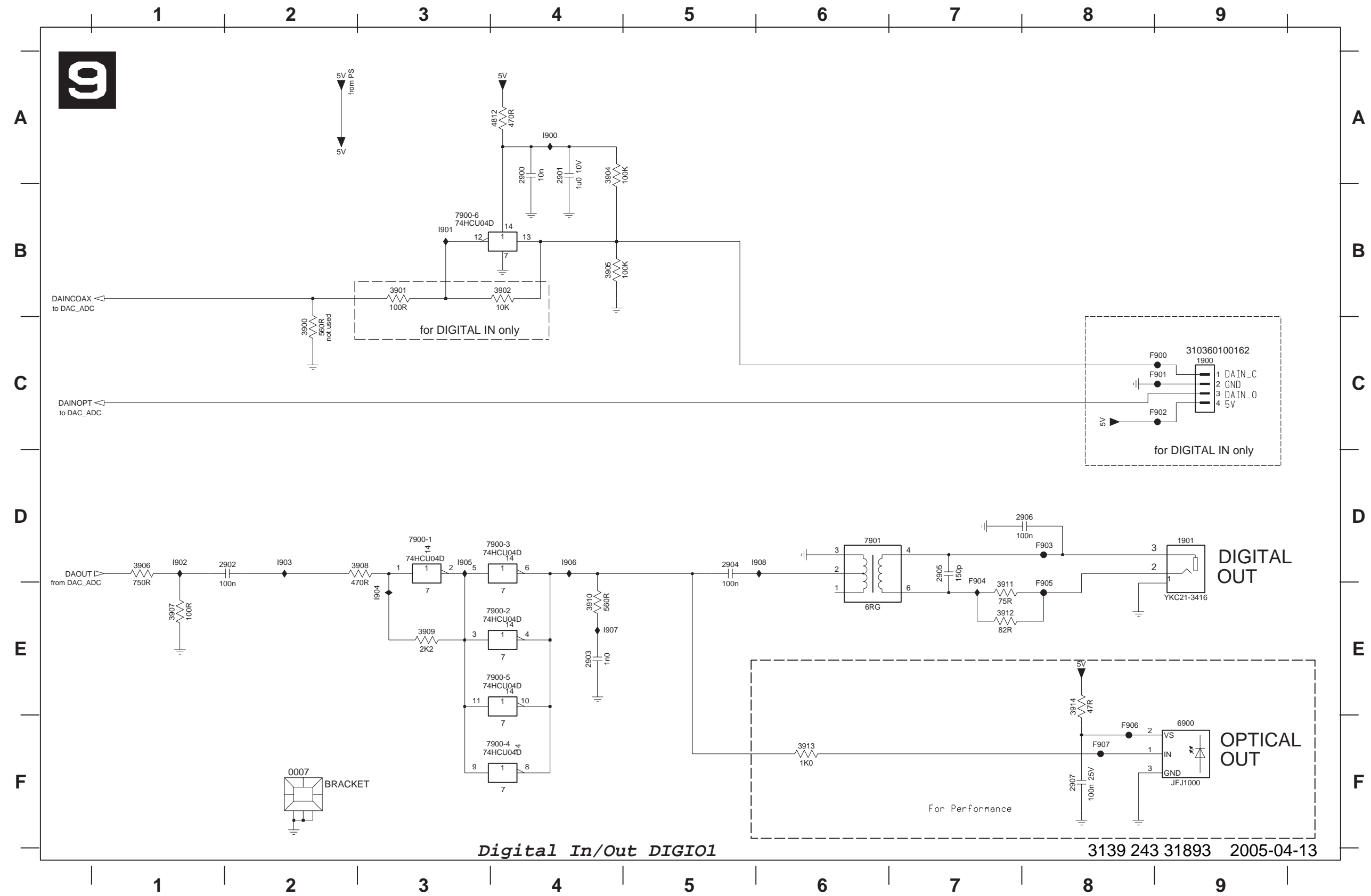
- 1500 F6
- 1522 D7
- 2500 A2
- 1523 E7
- 2501 C2
- 1524 D8
- 2502 C2
- 1525 E8
- 2503 D1
- 1526 D8
- 2504 D1
- 1527 F8
- 2505 E2
- 1528 E9
- 2506 E2
- 1529 F9
- 2507 F5
- 2508 F6
- 2509 F7
- 2510 A6
- 2511 A6
- 2512 A6
- 2513 A7
- 2514 A7
- 2515 C8
- 2516 B8
- 2517 C7
- 2518 C7
- 2519 D7
- 2520 D7
- 2521 E7
- 2522 E7
- 2523 D7
- 2524 E7
- 2525 E8
- 2526 F8
- 3501 B2
- 3502 B1
- 3503 D2
- 3504 D2
- 3505 E1
- 3506 E1
- 3507 E1
- 3508 E1
- 3509 A4
- 3510 A4
- 3511 A7
- 3512 A7
- 3513 B8
- 3514 D8
- 3515 E8
- 3516 E9
- 3517 E9
- 3518 A8
- 5500 F5
- 5501 B8
- 6500 B7
- 7500 A3
- 7501 A9
- 7502 E9
- 7503 F9
- 7504 A8
- 1500 B2
- 1501 B2
- 1502 C2
- 1503 C2
- 1504 D2
- 1505 D2
- 1506 D2
- 1507 D2
- 1508 E1
- 1509 E2
- 1510 E1
- 1511 E2
- 1512 A4
- 1513 A4
- 1514 A6
- 1515 A6
- 1516 A6
- 1517 B7
- 1518 B7
- 1519 B7
- 1521 D7

Analog: Audio Converter (DAC_ADC)



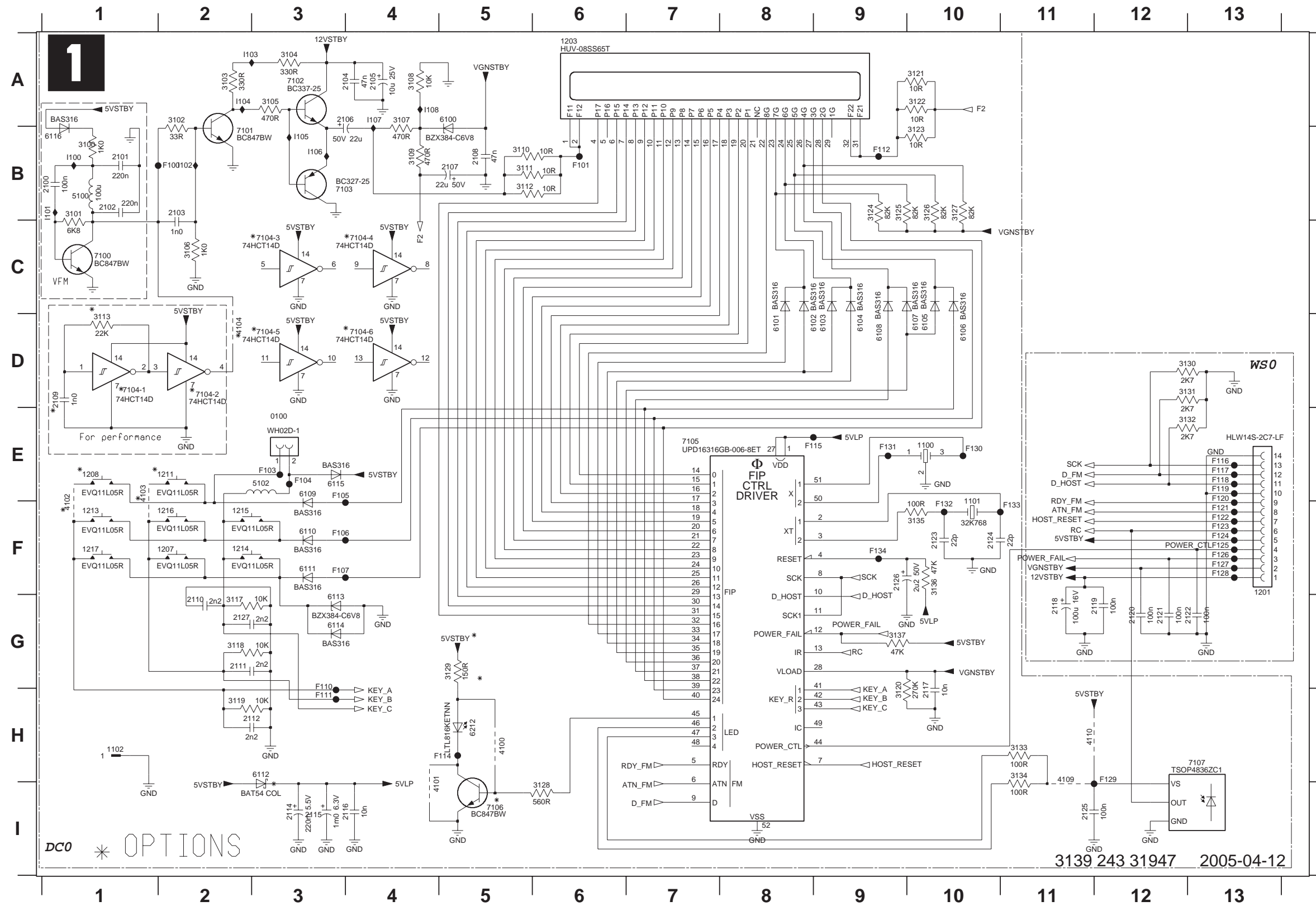
- 1700 E1
- 2700 B1
- 2701 B3
- 2702 D3
- 2703 D3
- 2704 D3
- 2705 D3
- 2706 E1
- 2707 E1
- 2708 F4
- 2709 F4
- 2710 E5
- 2711 E5
- 2712 D7
- 2713 C5
- 2714 B6
- 2715 B6
- 2716 A7
- 2717 B7
- 2718 B7
- 2719 B7
- 2720 B8
- 2721 B8
- 2722 B8
- 2723 C8
- 2724 C9
- 2725 D8
- 2726 D9
- 2727 D8
- 2728 E9
- 3700 B1
- 3701 B1
- 3702 A2
- 3703 C2
- 3706 D2
- 3707 D2
- 3708 D2
- 3709 D2
- 3710 D1
- 3711 D2
- 3712 D1
- 3713 E2
- 3714 E1
- 3715 E1
- 3716 A6
- 3717 C5
- 3718 C5
- 3719 C7
- 3720 B9
- 3721 B8
- 3722 C9
- 3723 C9
- 3724 D9
- 3725 D9
- 3726 D9
- 3727 E9
- 3728 D4
- 3729 F4
- 3730 F5
- 3731 C5
- 3736 A3
- 3737 B4
- 3738 B4
- 4700 B2
- 5700 A6
- 5701 D5
- 6700 B2
- 6701 B1
- 6703 C2
- 7700 A2
- 7701 A3
- 7702 C2
- 7703 B6
- 7704 D6
- 7705 B8
- 7706 C8
- 9014 F5
- F700 C1
- F701 C1
- F702 C1
- F703 D1
- F704 D1
- F705 D1
- F706 D1
- F707 D1
- F708 D1
- F709 D1
- F710 D1
- F711 E1
- F712 E1
- F713 A8
- I700 A1
- I701 A4
- I702 B2
- I703 E1
- I704 E1
- I705 D4
- I706 D3
- I707 D3
- I708 D3
- I709 E5
- I710 D6
- I711 E5
- I712 F5
- I713 F5
- I715 B8
- I716 C8
- I717 C8
- I718 D8
- I719 D9
- I720 D8
- I721 D9
- I722 C5
- I723 A6
- I724 F5
- c700 F9

Analog: Digital In / Out 1 (DIGIO 1)



- 0007 F2
- 1900 C9
- 1901 D9
- 2900 A4
- 2901 A4
- 2902 D2
- 2903 E4
- 2904 D5
- 2905 D7
- 2906 D8
- 2907 F8
- 3900 C2
- 3901 B3
- 3902 B4
- 3904 A4
- 3905 B4
- 3906 D1
- 3907 E1
- 3908 D3
- 3909 E3
- 3910 E4
- 3911 E7
- 3912 E7
- 3913 F6
- 3914 E8
- 4812 A4
- 6900 F9
- 7900-1 D3
- 7900-2 E4
- 7900-3 D4
- 7900-4 F4
- 7900-5 E4
- 7900-6 B3
- 7901 D6
- F900 C9
- F901 C9
- F902 C9
- F903 D8
- F904 D7
- F905 E8
- F906 F8
- F907 F8
- I900 A4
- I901 B3
- I902 D1
- I903 D2
- I904 E3
- I905 D3
- I906 D4
- I907 E4
- I908 D6

Front: Front Panel

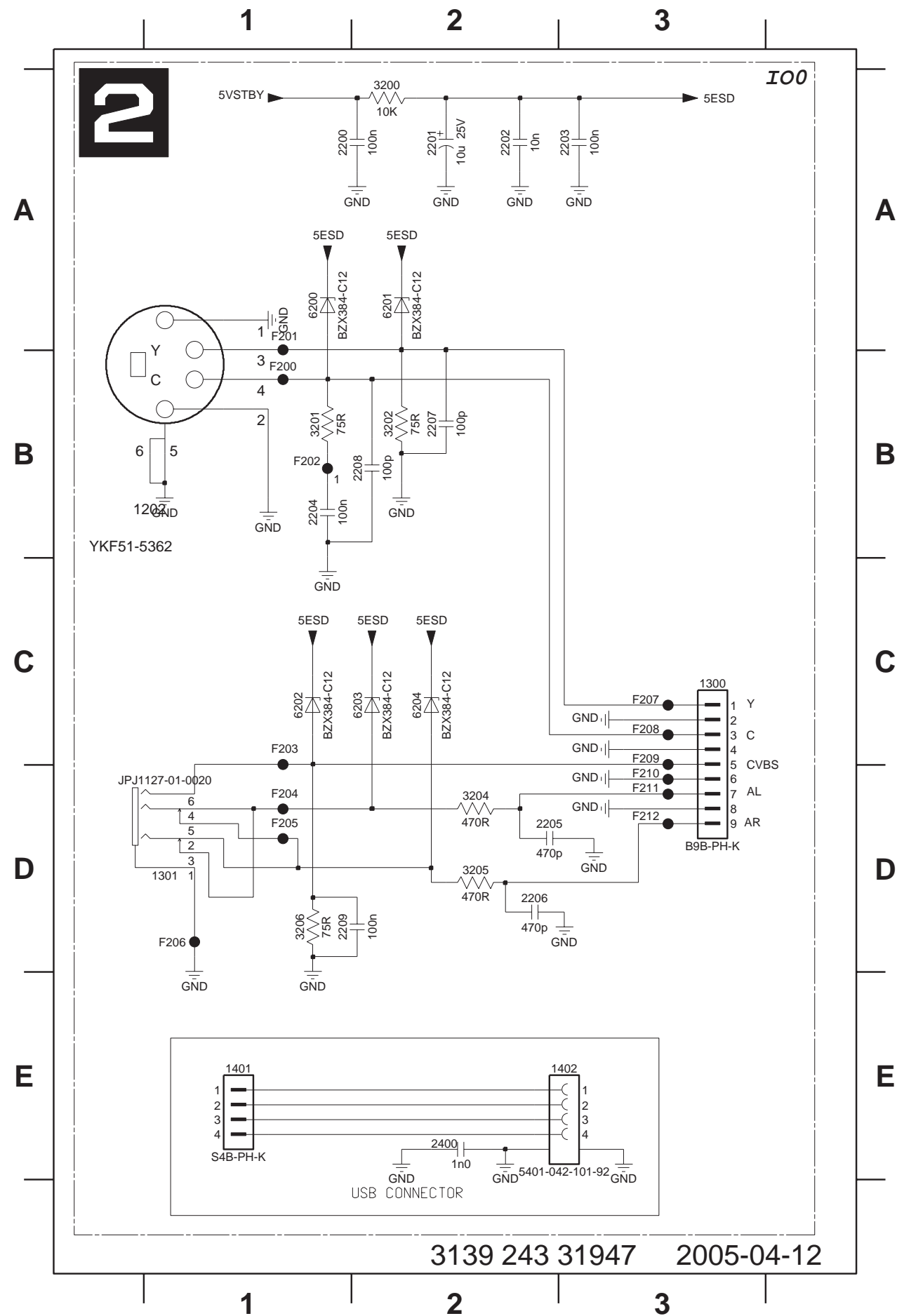


0100 E3	4101 I4	I107 A4
1100 E10	4102 F1	I108 A4
1101 F10	4103 E1	
1102 H1	4104 D2	
1201 F13	4109 H11	
1203 A6	4110 H11	
1207 F2	5100 B1	
1208 E1	5102 E3	
1211 E2	6100 A5	
1213 F1	6101 D8	
1214 F2	6102 D9	
1215 F2	6103 D9	
1216 F2	6104 D9	
1217 F1	6105 D10	
2100 B1	6106 D10	
2101 B1	6107 D10	
2102 B1	6108 D9	
2103 B2	6109 E3	
2104 A4	6110 F3	
2105 A4	6111 F3	
2106 A3	6112 H3	
2107 B5	6113 G3	
2108 B5	6114 G3	
2109 D1	6115 E3	
2110 G2	6116 B1	
2111 G2	6212 H5	
2112 H2	7100 C1	
2114 I3	7101 B2	
2115 I3	7102 A3	
2116 I4	7103 B3	
2117 H10	7104-1 D1	
2118 G11	7104-2 D2	
2119 G12	7104-3 C3	
2120 G12	7104-4 C4	
2121 G12	7104-5 D3	
2122 G13	7104-6 D4	
2123 F10	7105 E7	
2124 F10	7106 I5	
2125 I11	7107 H13	
2126 F9	F100 B2	
2127 G2	F101 B6	
3100 B1	F103 E3	
3101 B1	F104 E3	
3102 A2	F105 E3	
3103 A2	F106 F3	
3104 A3	F107 F3	
3105 A3	F110 H3	
3106 C2	F111 H3	
3107 A4	F112 B9	
3108 A4	F114 H5	
3109 B4	F115 E8	
3110 B5	F116 E13	
3111 B5	F117 E13	
3112 B5	F118 E13	
3113 D1	F119 E13	
3117 G2	F120 E13	
3118 G2	F121 F13	
3119 H2	F122 F13	
3120 H9	F123 F13	
3121 A10	F124 F13	
3122 A10	F125 F13	
3123 B10	F126 F13	
3124 B9	F127 F13	
3125 B9	F128 F13	
3126 B10	F129 H12	
3127 B10	F130 E10	
3128 I6	F131 E9	
3129 G5	F132 F10	
3130 D12	F133 F11	
3131 D12	F134 F9	
3132 E12	I100 B1	
3133 H11	I101 B1	
3134 H11	I102 B2	
3135 F10	I103 A2	
3136 F10	I104 A2	
3137 G9	I105 B3	
4100 H5	I106 B3	

3139 243 31947 2005-04-12

DC0 * OPTIONS

Front: Front Panel

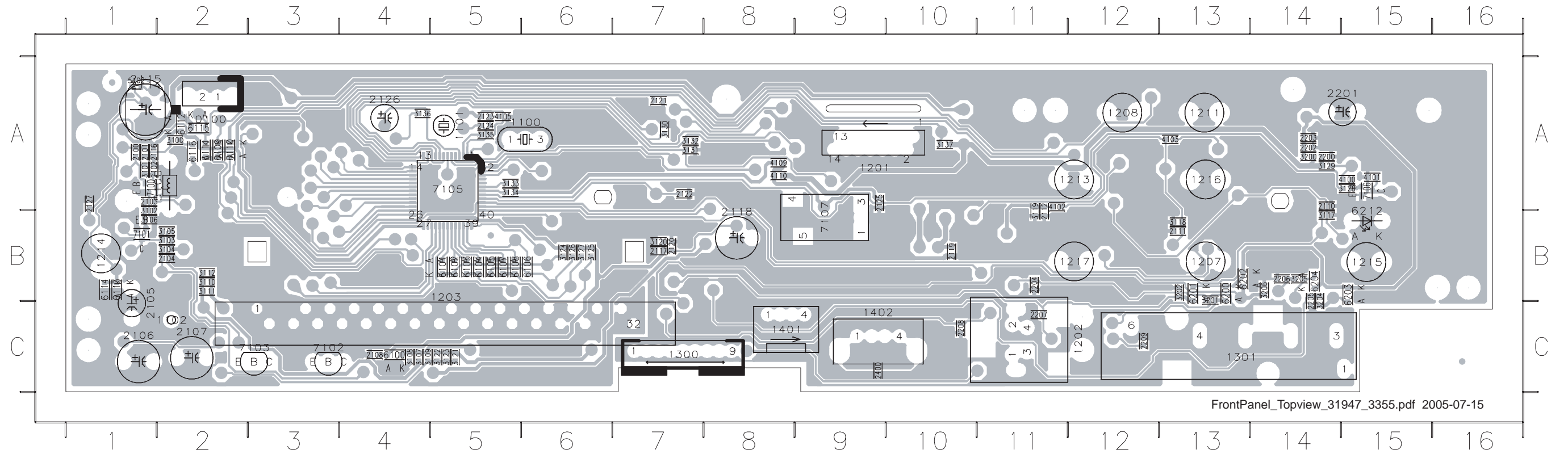


- 1202 B1
- 1300 C3
- 1301 D1
- 1401 E1
- 1402 E3
- 2200 A1
- 2201 A2
- 2202 A2
- 2203 A3
- 2204 B1
- 2205 D2
- 2206 D2
- 2207 B2
- 2208 B2
- 2209 D1
- 2400 E2
- 3200 A2
- 3201 B1
- 3202 B2
- 3204 D2
- 3205 D2
- 3206 D1
- 6200 A1
- 6201 A2
- 6202 C1
- 6203 C2
- 6204 C2
- F200 B1
- F201 A1
- F202 B1
- F203 C1
- F204 D1
- F205 D1
- F206 D1
- F207 C3
- F208 C3
- F209 C3
- F210 D3
- F211 D3
- F212 D3

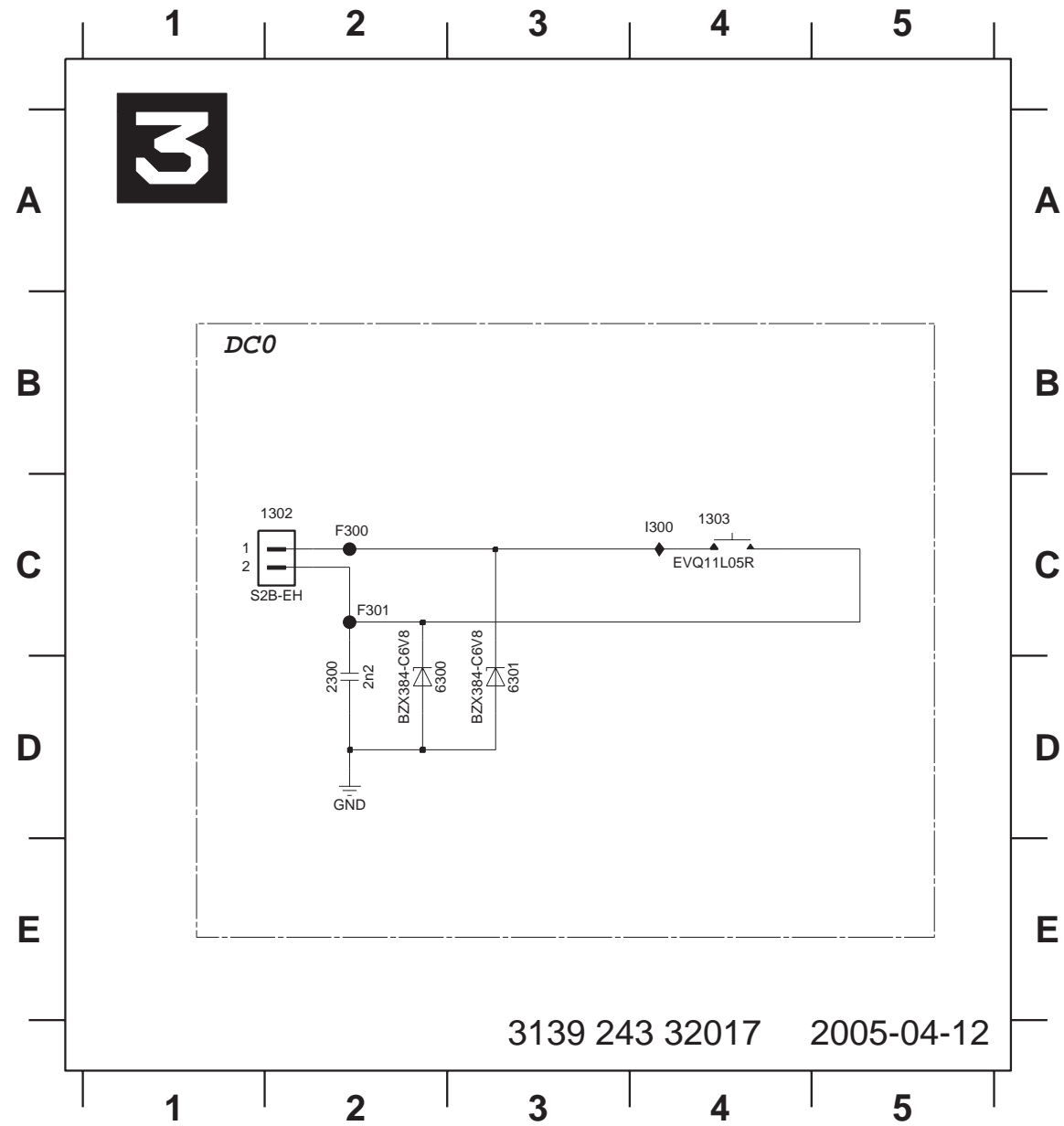
3139 243 31947 2005-04-12

Layout: Front Panel (Top View)

0100	A2	1211	A13	1402	C9	2108	C4	2119	B10	2200	A14	2200	A14	3107	C4	3120	B7	3129	A14	3200	A14	4103	A13	6103	B5	6112	A2	6204	B14
1100	A6	1213	A12	2100	A11	2110	A13	2120	B7	2201	A15	2202	A15	3108	C4	3121	B7	3130	A7	3201	B6	4104	A5	6104	B5	6113	B11	6205	B15
1101	A5	1214	B12	2101	A11	2111	B13	2121	A7	2203	A14	2204	A14	3109	C4	3122	B7	3131	A7	3202	B6	4105	A8	6105	B5	6114	B11	6206	B15
1102	C2	1215	B13	2102	A11	2112	B11	2122	A7	2205	A14	2206	A14	3110	C4	3123	B7	3132	A7	3203	B6	4106	A2	6106	B5	6115	B11	6207	B15
1201	A9	1216	B13	2103	A11	2113	A1	2123	A5	2207	A14	2208	A14	3111	C4	3124	B7	3133	A7	3204	B6	4107	A1	6107	B5	6116	B11	6208	B15
1202	C12	1217	B12	2104	B2	2114	A1	2124	A5	2209	B11	2210	B11	3112	C4	3125	B7	3134	A5	3205	B6	4108	A1	6108	B5	6117	B11	6209	B15
1203	B5	1300	C7	2105	C1	2115	A1	2125	A9	2211	B11	2212	B11	3113	C4	3126	B7	3135	A5	3206	B6	4109	A1	6109	B5	6118	B11	6210	B15
1207	B13	1301	C13	2106	C1	2116	B7	2126	A4	2213	C10	2214	C10	3114	C4	3127	B7	3136	A4	3207	B6	4110	A1	6110	B5	6119	B11	6211	B15
1208	A12	1401	C8	2107	C2	2117	B8	2127	A1	2215	C10	2216	C10	3115	C4	3128	B7	3137	A10	3208	B6	4111	A1	6111	B5	6120	B11	6212	B15

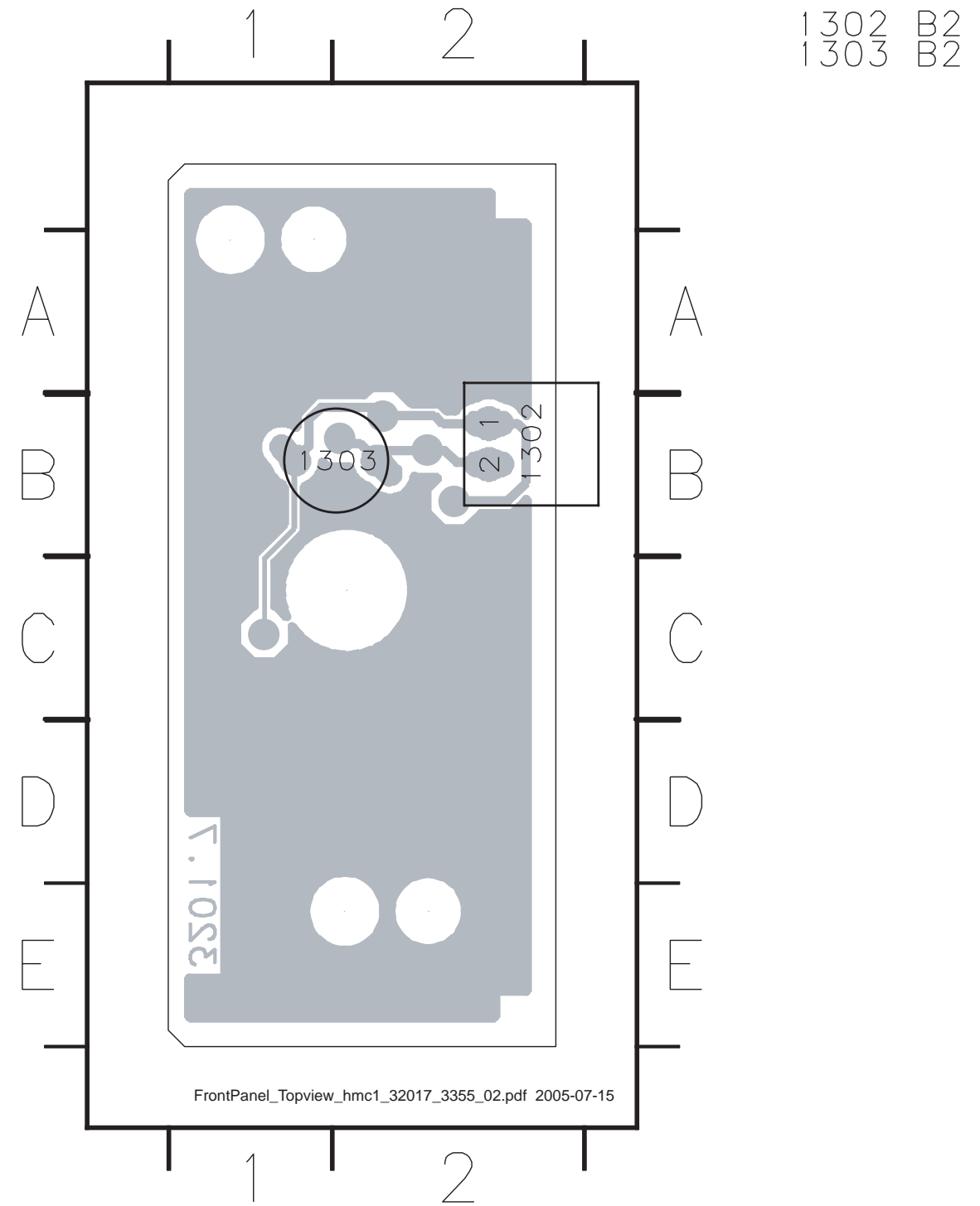


Front: Standby



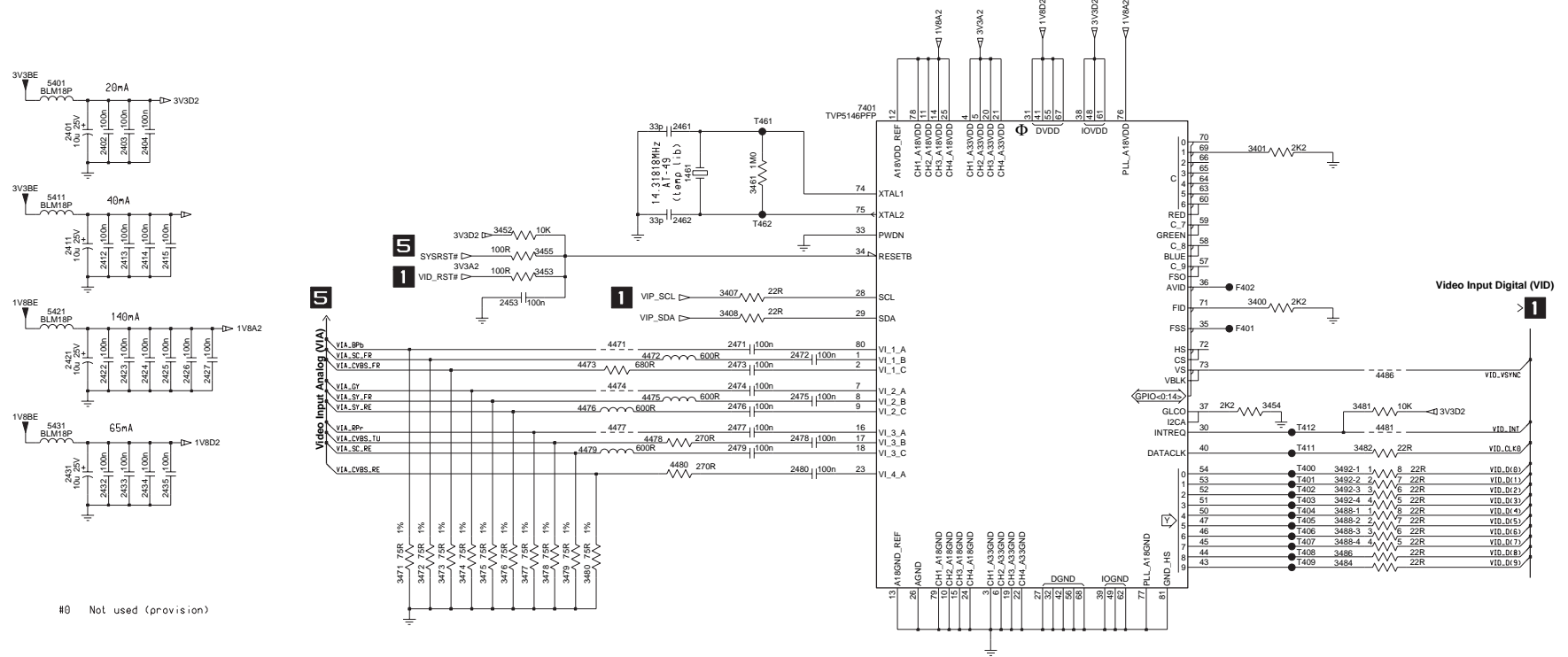
- 1302 C2
- 1303 C4
- 2300 D2
- 6300 D2
- 6301 D3
- F300 C2
- F301 C2
- I300 C4

Layout: Standby (Top View)



Digital: Video Input Processor

4 Video Input Processor



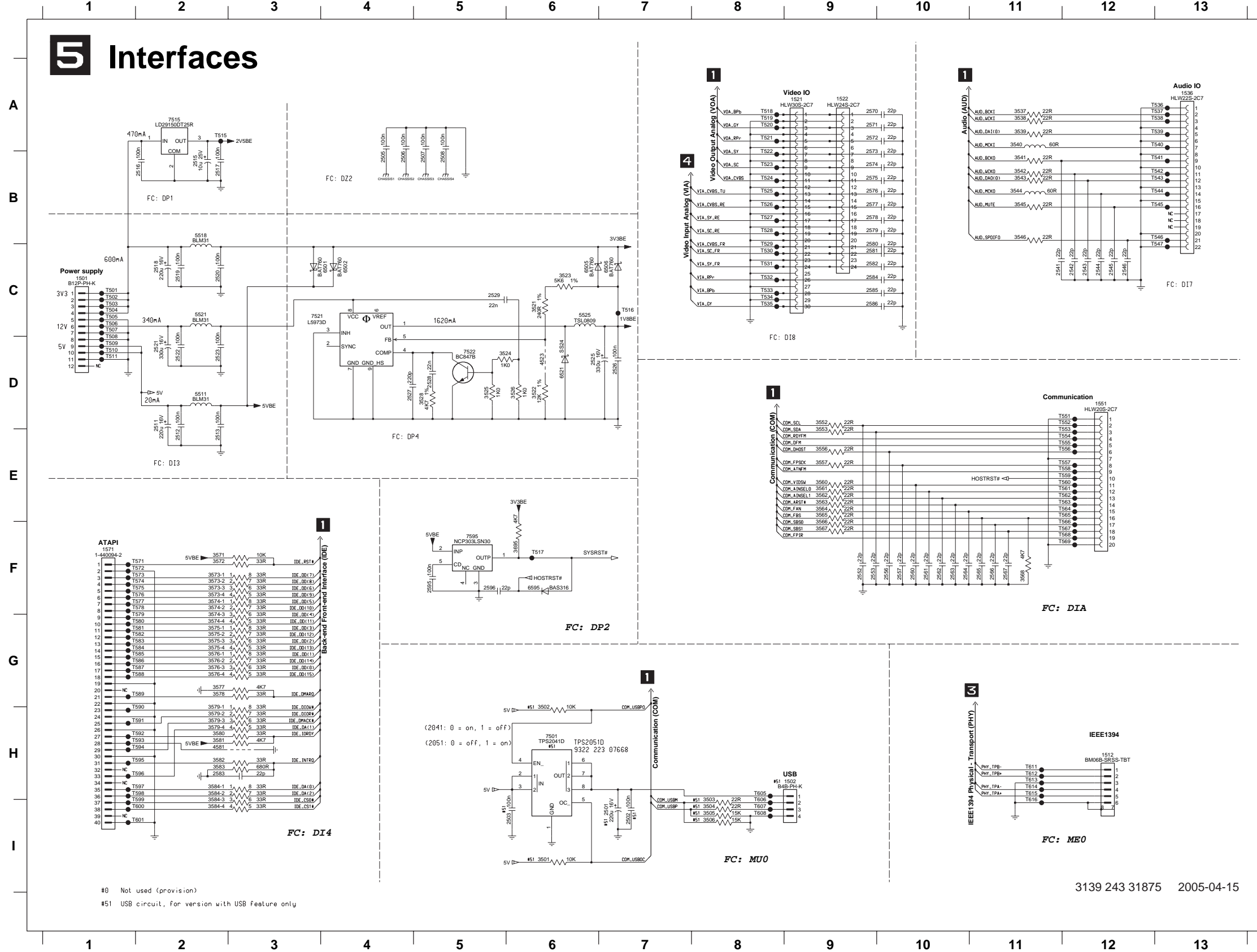
#0 Not used (provision)

FC: D18

- 1461 C6
- 2401 C2
- 2402 C2
- 2403 C2
- 2404 C2
- 2411 D2
- 2412 D2
- 2413 D2
- 2414 D2
- 2415 D2
- 2421 E2
- 2422 E2
- 2423 E2
- 2424 E2
- 2425 E2
- 2426 E3
- 2427 E3
- 2431 E2
- 2432 E2
- 2433 F2
- 2434 F2
- 2435 F2
- 2453 D5
- 2461 C6
- 2462 D6
- 2471 E6
- 2472 E7
- 2473 E6
- 2474 E6
- 2475 E7
- 2476 E6
- 2477 E6
- 2478 E7
- 2479 E6
- 2480 E7
- 3400 D10
- 3401 C10
- 3407 D6
- 3408 D6
- 3452 D5
- 3453 D5
- 3454 E10
- 3455 D5
- 3461 C7
- 3471 F4
- 3472 F4
- 3473 F4
- 3474 F5
- 3475 F5
- 3476 F5
- 3477 F5
- 3478 F5
- 3479 F5
- 3480 F5
- 3481 E11
- 3482 E11
- 3484 F11
- 3486 F11
- 3488-1 F11
- 3488-2 F11
- 3488-3 F11
- 3488-4 F11
- 3492-1 E11
- 3492-2 F11
- 3492-3 F11
- 3492-4 F11
- 4471 E6
- 4472 E6
- 4473 E5
- 4474 E6
- 4475 E6
- 4476 E5
- 4477 E6
- 4478 E6
- 4479 E5
- 4480 E6
- 4481 E11
- 4486 E11
- 5401 C2
- 5411 D2
- 5421 D2
- 5431 E2
- 7401 C7
- F401 D10
- F402 D10
- T400 E10
- T401 F10
- T402 F10
- T403 F10
- T404 F10
- T405 F10
- T406 F10
- T407 F10
- T408 F10
- T409 F10
- T411 E10
- T412 E10
- T461 C7
- T462 D7

Digital: Interfaces

5 Interfaces

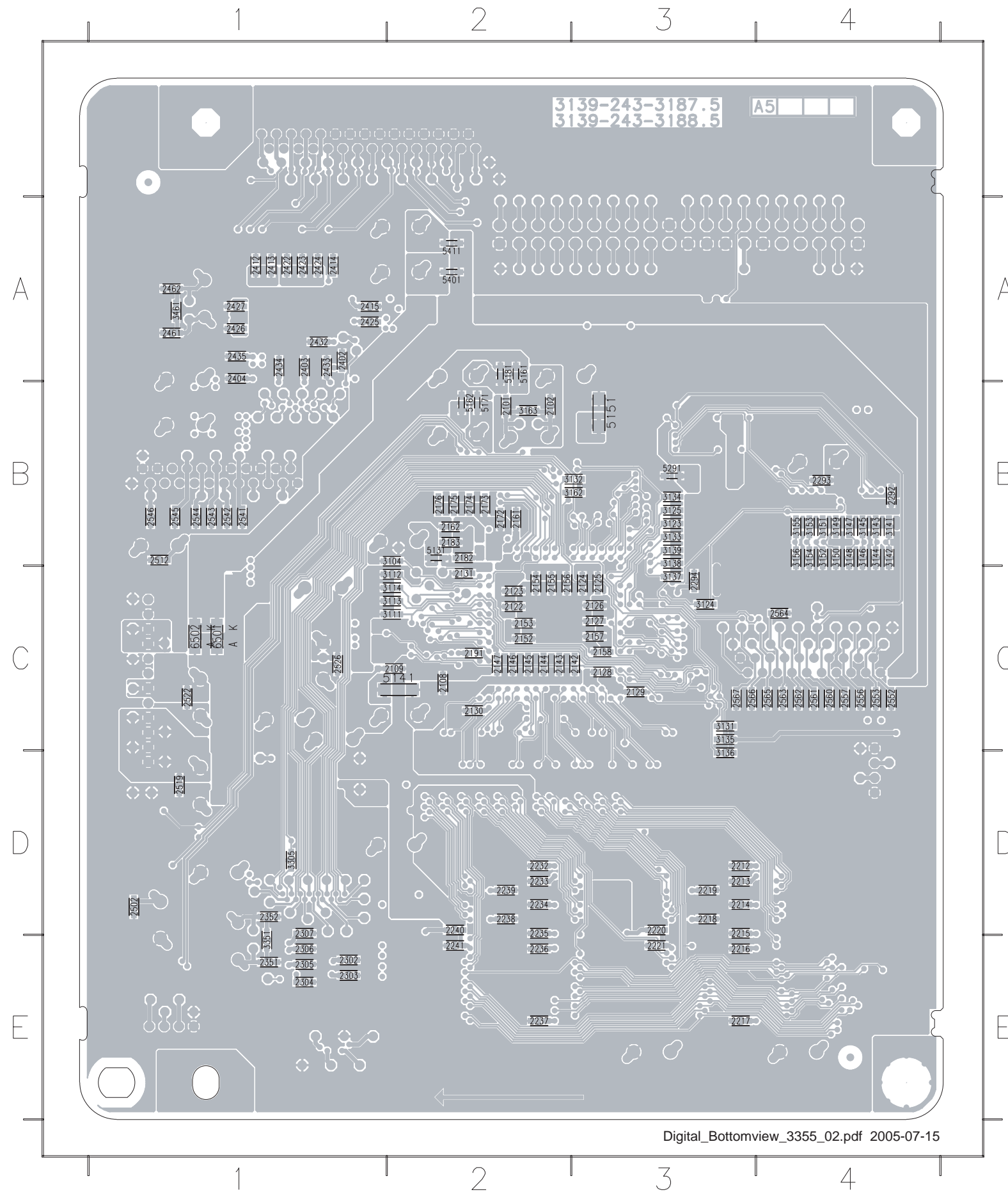


1501 C1	3575-3 G2	T587 G1
1502 H9	3575-4 G2	T588 G1
1512 H12	3576-1 G2	T589 G1
1521 A9	3576-2 G2	T590 H1
1522 A9	3576-3 G2	T591 H1
1536 A13	3576-4 G2	T592 H1
1551 D12	3577 G2	T593 H1
1571 F1	3578 G2	T594 H1
2501 I7	3579-1 H2	T595 H1
2502 I7	3579-2 H2	T596 H1
2503 I6	3579-3 H2	T597 H1
2505 B4	3579-4 H2	T598 H1
2506 B4	3580 H2	T599 I1
2507 B5	3581 H2	T600 I1
2508 B5	3582 H2	T601 H1
2511 D2	3583 H2	T605 H8
2512 E2	3584-1 H2	T606 I8
2513 E2	3584-2 H2	T607 I8
2515 B2	3584-3 I2	T608 I8
2516 B2	3584-4 I2	T611 H11
2517 B2	3585 F6	T612 H11
2518 C2	4523 D6	T613 H11
2519 C2	4581 H2	T614 H11
2520 C2	5511 D2	T615 H11
2521 D2	5518 B2	
2522 D2	5521 C2	
2523 D2	5525 C2	
2525 D6	6501 C4	
2526 D7	6502 C4	
2527 D4	6505 C6	
2528 D5	6506 C7	
2529 C5	6521 D6	
2531 C11	6525 C11	
2542 C12	7501 H6	
2543 C12	7515 A2	
2544 C12	7521 C3	
2545 C12	7522 D5	
2546 C12	7525 F5	
2552 F9	7501 C1	
2553 F9	7502 C1	
2556 F10	7503 C1	
2557 F10	7504 C1	
2560 F10	7505 C1	
2561 F10	7506 C1	
2562 F10	7507 C1	
2563 F10	7508 D1	
2564 F10	7509 D1	
2565 F11	7510 D1	
2566 F11	7511 D1	
2567 F11	7515 A2	
2570 A9	7516 C7	
2571 A9	7517 F6	
2572 A9	7518 A8	
2573 B9	7519 A8	
2574 B9	7520 A8	
2575 B9	7521 A8	
2576 B9	7522 B8	
2577 B9	7523 B8	
2578 B9	7524 B8	
2579 B9	7525 B8	
2580 C9	7526 B8	
2581 C9	7527 B8	
2582 C9	7528 B8	
2583 H2	7529 C8	
2584 C9	7530 C8	
2585 C9	7531 C8	
2586 C9	7532 C8	
2589 F5	7533 C8	
2596 F5	7534 C8	
3501 I6	7535 C8	
3502 H6	7536 A13	
3503 I8	7537 A13	
3504 I8	7538 A13	
3505 I8	7539 A13	
3506 I8	7540 A13	
3521 C6	7541 B13	
3522 D6	7542 B13	
3523 C6	7543 B13	
3524 D6	7544 B13	
3525 D5	7545 B13	
3526 D6	7546 B13	
3528 D5	7547 C13	
3537 A11	7551 D12	
3538 A11	7552 D12	
3539 A11	7553 D12	
3540 A11	7554 E12	
3541 B11	7555 E12	
3542 B11	7556 E12	
3543 B11	7557 E12	
3544 B11	7558 E12	
3545 B11	7559 E12	
3546 B11	7560 E12	
3552 D9	7561 E12	
3553 E9	7562 E12	
3556 E9	7563 E12	
3557 E9	7564 E12	
3560 E9	7565 E12	
3561 E9	7566 F12	
3562 E9	7567 F12	
3563 E9	7568 F12	
3564 E9	7569 F12	
3565 E9	7571 F1	
3566 F9	7572 F1	
3567 F9	7573 F1	
3568 F11	7574 F1	
3571 F2	7575 F1	
3572 F2	7576 F1	
3573-1 F2	7577 F1	
3573-2 F2	7578 F1	
3573-3 F2	7579 G1	
3573-4 F2	7580 G1	
3574-1 F2	7581 G1	
3574-2 F2	7582 G1	
3574-3 G2	7583 G1	
3574-4 G2	7584 G1	
3575-1 G2	7585 G1	
3575-2 G2	7586 G1	

3139 243 31875 2005-04-15

#0 Not used (provision)
#51 USB circuit, for version with USB feature only

Layout: Digital-Main Part (Bottom View)



2101	B2
2102	B2
2108	B2
2109	B2
2123	B2
2124	B2
2125	B2
2126	B2
2127	B2
2128	B2
2129	B2
2130	B2
2131	B2
2132	B2
2133	B2
2134	B2
2135	B2
2136	B2
2137	B2
2138	B2
2139	B2
2140	B2
2141	B2
2142	B2
2143	B2
2144	B2
2145	B2
2146	B2
2147	B2
2148	B2
2149	B2
2150	B2
2151	B2
2152	B2
2153	B2
2154	B2
2155	B2
2156	B2
2157	B2
2158	B2
2159	B2
2160	B2
2161	B2
2162	B2
2163	B2
2164	B2
2165	B2
2166	B2
2167	B2
2168	B2
2169	B2
2170	B2
2171	B2
2172	B2
2173	B2
2174	B2
2175	B2
2176	B2
2177	B2
2178	B2
2179	B2
2180	B2
2181	B2
2182	B2
2183	B2
2184	B2
2185	B2
2186	B2
2187	B2
2188	B2
2189	B2
2190	B2
2191	B2
2192	B2
2193	B2
2194	B2
2195	B2
2196	B2
2197	B2
2198	B2
2199	B2
2200	B2
2201	B2
2202	B2
2203	B2
2204	B2
2205	B2
2206	B2
2207	B2
2208	B2
2209	B2
2210	B2
2211	B2
2212	B2
2213	B2
2214	B2
2215	B2
2216	B2
2217	B2
2218	B2
2219	B2
2220	B2
2221	B2
2222	B2
2223	B2
2224	B2
2225	B2
2226	B2
2227	B2
2228	B2
2229	B2
2230	B2
2231	B2
2232	B2
2233	B2
2234	B2
2235	B2
2236	B2
2237	B2
2238	B2
2239	B2
2240	B2
2241	B2
2242	B2
2243	B2
2244	B2
2245	B2
2246	B2
2247	B2
2248	B2
2249	B2
2250	B2
2251	B2
2252	B2
2253	B2
2254	B2
2255	B2
2256	B2
2257	B2
2258	B2
2259	B2
2260	B2
2261	B2
2262	B2
2263	B2
2264	B2
2265	B2
2266	B2
2267	B2
2268	B2
2269	B2
2270	B2
2271	B2
2272	B2
2273	B2
2274	B2
2275	B2
2276	B2
2277	B2
2278	B2
2279	B2
2280	B2
2281	B2
2282	B2
2283	B2
2284	B2
2285	B2
2286	B2
2287	B2
2288	B2
2289	B2
2290	B2
2291	B2
2292	B2
2293	B2
2294	B2
2295	B2
2296	B2
2297	B2
2298	B2
2299	B2
2300	B2
2301	B2
2302	B2
2303	B2
2304	B2
2305	B2
2306	B2
2307	B2
2308	B2
2309	B2
2310	B2
2311	B2
2312	B2
2313	B2
2314	B2
2315	B2
2316	B2
2317	B2
2318	B2
2319	B2
2320	B2
2321	B2
2322	B2
2323	B2
2324	B2
2325	B2
2326	B2
2327	B2
2328	B2
2329	B2
2330	B2
2331	B2
2332	B2
2333	B2
2334	B2
2335	B2
2336	B2
2337	B2
2338	B2
2339	B2
2340	B2
2341	B2
2342	B2
2343	B2
2344	B2
2345	B2
2346	B2
2347	B2
2348	B2
2349	B2
2350	B2
2351	B2
2352	B2
2353	B2
2354	B2
2355	B2
2356	B2
2357	B2
2358	B2
2359	B2
2360	B2
2361	B2
2362	B2
2363	B2
2364	B2
2365	B2
2366	B2
2367	B2
2368	B2
2369	B2
2370	B2
2371	B2
2372	B2
2373	B2
2374	B2
2375	B2
2376	B2
2377	B2
2378	B2
2379	B2
2380	B2
2381	B2
2382	B2
2383	B2
2384	B2
2385	B2
2386	B2
2387	B2
2388	B2
2389	B2
2390	B2
2391	B2
2392	B2
2393	B2
2394	B2
2395	B2
2396	B2
2397	B2
2398	B2
2399	B2
2400	B2
2401	B2
2402	B2
2403	B2
2404	B2
2405	B2
2406	B2
2407	B2
2408	B2
2409	B2
2410	B2
2411	B2
2412	B2
2413	B2
2414	B2
2415	B2
2416	B2
2417	B2
2418	B2
2419	B2
2420	B2
2421	B2
2422	B2
2423	B2
2424	B2
2425	B2
2426	B2
2427	B2
2428	B2
2429	B2
2430	B2
2431	B2
2432	B2
2433	B2
2434	B2
2435	B2
2436	B2
2437	B2
2438	B2
2439	B2
2440	B2
2441	B2
2442	B2
2443	B2
2444	B2
2445	B2
2446	B2
2447	B2
2448	B2
2449	B2
2450	B2
2451	B2
2452	B2
2453	B2
2454	B2
2455	B2
2456	B2
2457	B2
2458	B2
2459	B2
2460	B2
2461	B2

Notes:

8. Circuit- and IC description

8.1. Front Board (Panel – Display + Key)

8.1.1. General

This board consists of the following parts:

- Slave μ P
- Frontend (Audio & Video)
- VFD Heater voltage Generator

8.1.2. Slave μ P (IC 7105: UPD16316GB)

The core element of the Front Display + Keyboard is the slave μ P. It runs on a 5V supply and is responsible for the following functions:

- Interface with the Domino chip on the Digital Board
- Evaluation of the keyboard matrix within Front board
- Decoding the remote control commands from the infra-red receiver
- Activation and control of the display
- Timer Wake-up activation

It runs on two clock frequencies namely:

- 5MHz for normal operation
- 32.768KHz for the real time clock

8.1.3. Interface to the Domino chip

It communicates with the Domino Host on the Digital board via a 6-wire synchronous serial interface. The Host is always the master to generate the communication clock to the slave μ P irrespective of the direction of data transfer.

8.1.4. Evaluation of the keyboard matrix

A key matrix is used on the Front board. The slave μ P does the key scanning with FIP9 - FIP24 (pin 23-26 and 29-40) as output and KEY_A - KEY_C (pin 41-43) as input. Each key is assigned a key code based on the output and input ports, and the slave μ P will do the evaluation by getting the key codes.

8.1.5. IR receiver and signal evaluation

The IR receiver on the Front Board contains a selectively controlled amplifier as well as a photodiode. The photo-diode changes the received infrared transmission to electrical pulses, which are then amplified and demodulated. On the output of the IR receiver, a pulse sequence with TTL-level, which corresponds to the envelope curve of the received IR remote control command, can be measured. This pulse sequence is fed into the slave μ P for further processing via pin 13.

8.1.6. Vacuum Fluorescent Display [1203: HUV-08SS65T]

The VFD is fully controlled and driven by the slave μ P.

8.1.7. VFD Heater Voltage Generator

The oscillator circuit provided by [5100, 2101, 2102 & 7100] provides the necessary sine wave signal for transistors [7101, 7102 & 7103] to generate the 50% duty-cycle 48KHz AC square-wave signal for the filament of the VFD.

8.1.8. Timer Wake-up activation

During the Standby mode, the slave μ P provides a wakeup call (POWER_CTL-line switches to high) to the Domino Host on the Digital Board. It will then starts up and asks for the wake-up reason.

8.2. Analog Board

8.2.1. General

The pc board consist of the following parts:

- Fan Control (OPTION)
- Power Supply Unit
- Tuner Frontend
- Audio ADC/DAC

8.2.2. Fan Control

The Laser on the OPU of the drive is very sensitive to temperature. A fan control circuit [7802 & 7803] is built into the board as a provision. The fan is ON when the set is in active mode, and OFF when the tray opens. When the set is in Standby mode, the fan is switched off. The control of the fan is coming from the Digital Board.

8.2.3. Power Supply Unit

This power supply functions on a circuitry combination of a SMPS control IC [7400], switching FET [7401] and transformer [5400] as a switched-mode power supply (SMPS).

Feedback control is provided by the IC 7404, which compares the 5V-output voltage via voltage dividers [3421, 3422 & 3423] with an internal 2.5V reference voltage. The output voltage is fed to an optocoupler [7403] that provide the insulation between the primary and secondary parts as a current value into pin 3 of the IC 7400.

The following are the various supply lines provided:

- 3V3SW to CU, DAC_ADC, Digital Board
- 5V to IOA, IOV, CU, CINCH, MSP, DIGIO and FV
- 5N to MSP (provision only) and Digital Board (provision only)
- 5VE to Basic Engine
- 5V_BE to Digital Board
- 5NSTBY to IOA, CINCH and DAC_ADC
- 5VSTBY to IOA, IOV, FV, MSP, DAC_ADC, Front Board
- 8VSTBY to MSP
- 12V to Digital Board
- 12VSTBY to CU, IOV, DAC_ADC, Front Board
- 12VE to Basic Engine and Digital Board (provision only)
- 33VSTBY to FV
- VGNSTBY to Front Board

Standby modes:

In Standby mode, the STBY control line is low, switching off the 3V3SW, 5V, 5N (provision), 5VE, 12V and 12VE supply and thus reducing the power consumption.

8.2.4. Tuner Frontend [1100 : TMQZ2]

It has a RF IN for antenna connection and RF OUT which provides a RF loop through for connection to the TV.

The Frontend (Tuner & IF-demodulator) is controlled by I²C (SCL_5V- and SDA_5V-) lines coming from the Domino Host on the Digital board.

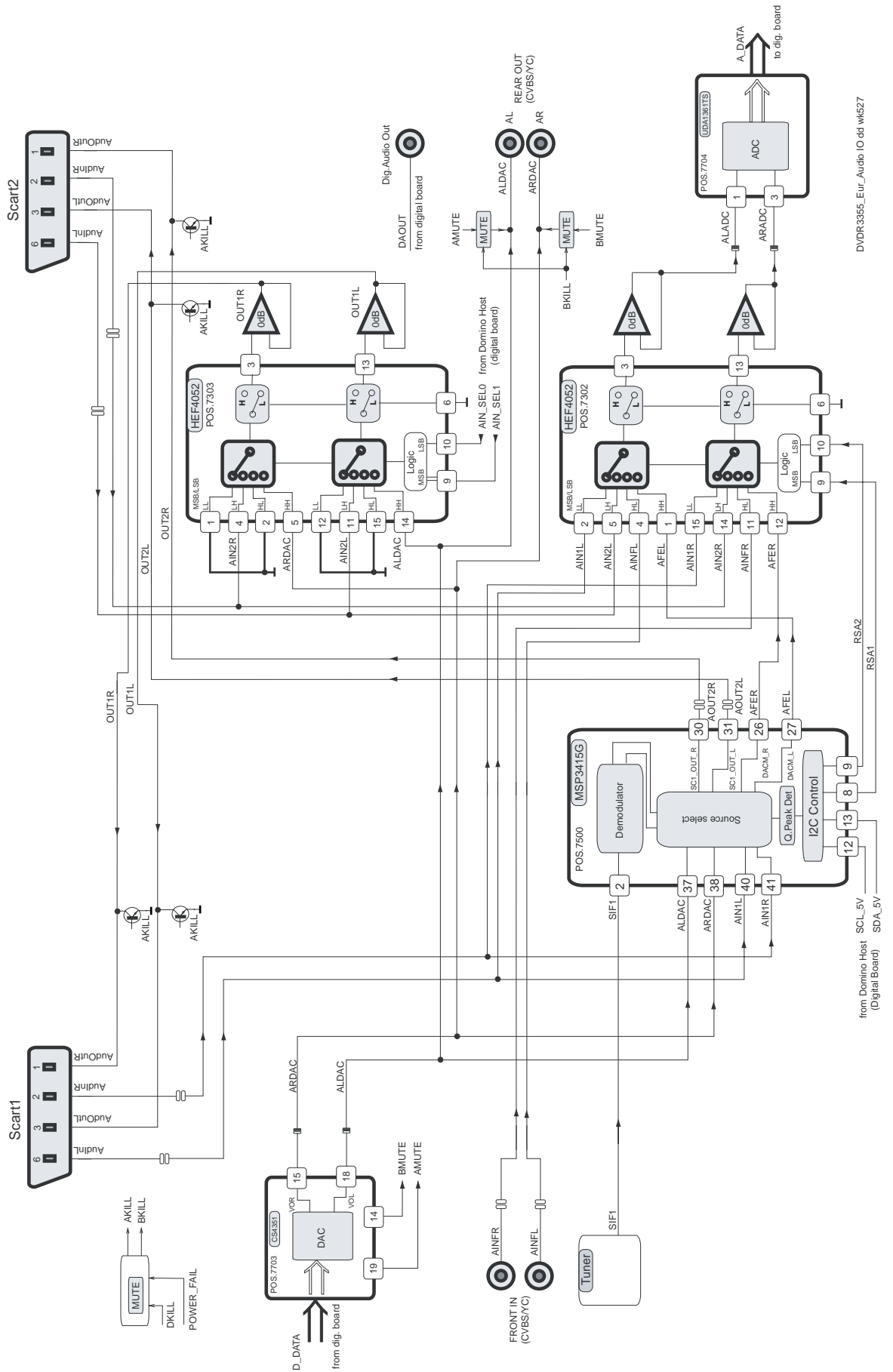
Complete video processing is done in this unit and the video output (CVBS) is taken out from the [VID_OUT] pin via a transistor as CVBS_TV-line to the Video I/O circuitry. The audio-IF component SIF1 is taken out from the [SIFOUT] pin for the demodulation by the Multi-sound processor (MSP).

Audio demodulator

The sound demodulation is done by the MSP3415 [7500], which is also fully controlled via I²C bus by the Domino Host. The audio signals are available at pin 26 and pin 27 and fed as AFER- & AFEL- line to the audio I/O for further processing.

8.2.5. Audio routing

Analog Audio In / Out Overview



DVDR.3355_Eur_Audio IO dd wk627

from Domino Host (Digital Board) SCL_5V SDA_5V RSA1 RSA2

Figure 8-1 Analog Audio In / Out Overview

The sound processing is always done in stereo (that means separate left- and right- channel) and the complete switching is realized by using HEF4052 which is a dual four-to-one multiplexer and MSP3415G which is a multi-sound processor.

a) Scart 1 – Output path

The multiplexer [7303] selects either signals from the Scart 2 Input (AIN2L/AIN2R) or the Audio DAC (ALDAC/ARDAC) as the output source for Scart 1 (AOUT1L/AOUT1R).

b) Scart 2 – Output path

The MSP [7500] selects either signals from the Scart 1 Input (AIN1L/AIN1R), the Audio DAC (ALDAC/ARDAC) or the Tuner Frontend as the output source for Scart 2 (AOUT2L/AOUT2R).

c) Digital audio-out path

In addition, a digital output (DAOUT) coming from the Digital board is passed through a 6-fold inverter [7900] for performance reasons (noise reduction, jitter, ...) and transformer (level correction, ground isolation,...) to the digital out cinch socket at the rear.

d) Record path

The record-selector [7302] selects either signals from the Scart 1 Input (AIN1L/AIN1R), Scart 2 Input (AIN2L/AIN2R), Front Cinch (AINFL/AINFR) or the MSP (AFEL/AFER) and routes to the audio ADC (ALADC/ARADC) for record purposes. The switch is controlled via RSA1 and RSA2 signals coming from the MSP.

8.2.6. Audio ADC/DAC

The conversion of analog audio signals from the record-selector [7302] outputs (ALADC/ARADC) is done via UDA1361TS [7704]. This IC can process input signals up to 2Vrms by using external resistors in series to the input pins. All required clock signals are generated on the digital board and only the audio data (A_DAT-line) are routed to Digital board for further processing.

The transformation of digital audio back into analog domain is done by CS4351 [7703]. All necessary clock signals are coming from the digital board and digital audio data (D_DATA0-line) are converted into analog signals (pin 15 and 18). The output signals from the audio DAC part (ALDAC/ARDAC) are directly routed to the rear cinch sockets. To avoid plops and any other audible noise on the output muting circuits are implemented for each channel. Muting for the various other output lines are done via AKILL & BKILL-lines which is a combination of the D_KILL from the Digital board and POWER_FAIL from power supply and AMUTE & BMUTE (digital silence mute) from DAC-part.

8.2.7. Video-routing

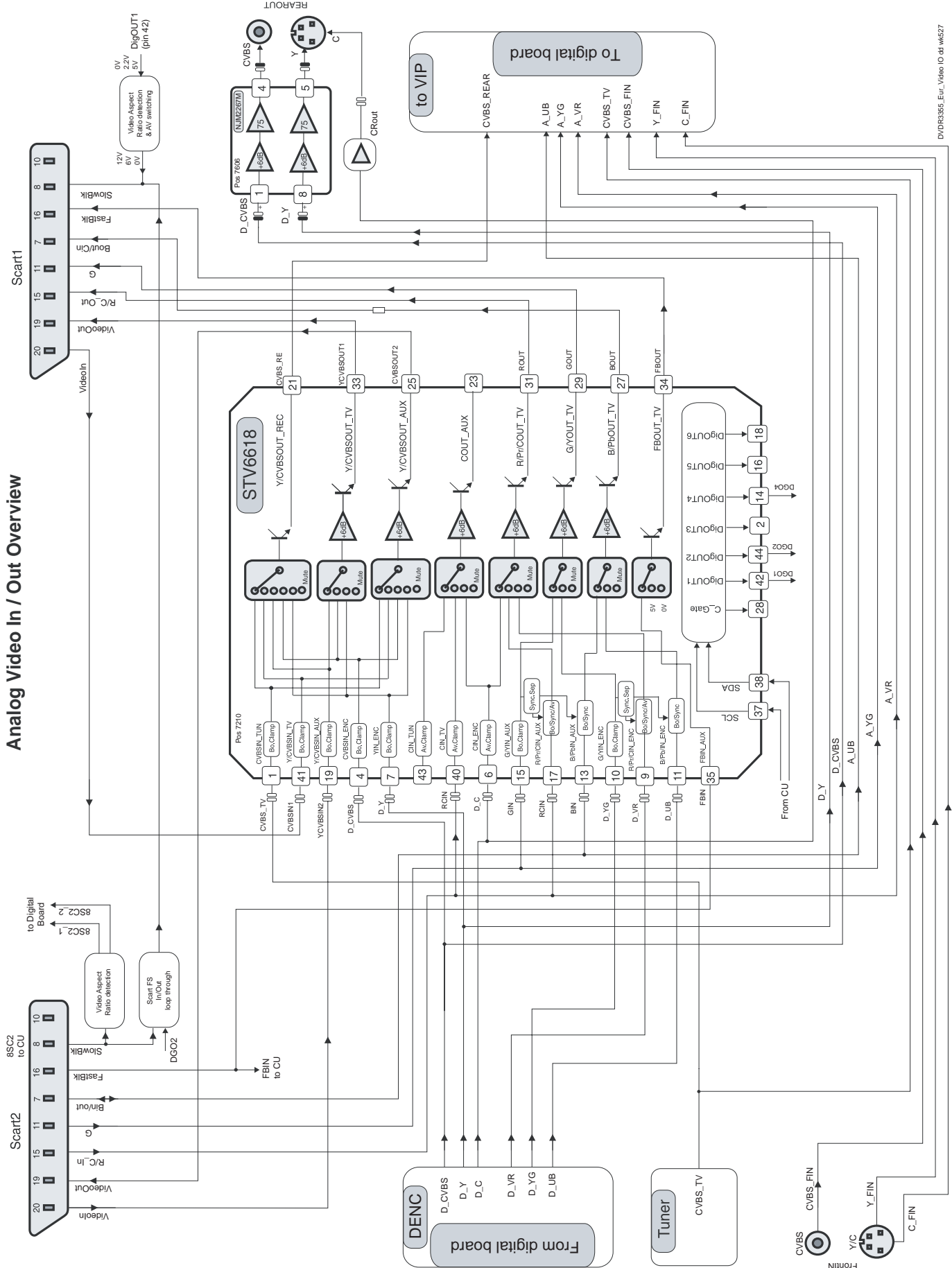


Figure 8-2 Analog Video In / Out Overview

A matrix switch STV6618 [7210] controlled by the Domino Host via I²C-bus is used for Video I/O switching. All used outputs excluding pin 21 (Y/CVBS-REC) have a 6dB-amplification and a 75 ohms-driver-stage inside. This IC also includes several digital outputs, which are used for switching purposes on the Analog board.

This matrix switch routes the selected inputs to the correct output lines for TV viewing and further processing in the Digital board.

The record selector inside the switch selects between the inputs from Tuner Frontend (CVBS_TV), CVBS Scart1 (CVBSIN1), CVBS Scart2 (CVBSIN2) or D_CVBS from the DENC (on Digital board). The output signal CVBS_RE together with the other signals CVBS_FIN, Y_FIN & C_FIN from the Front and RCB from Scart2 are routed directly to the VIP (on Digital board) for further processing.

The signals D_C and D_Y are fed through [7606] (6dB amplification) and D_C via transistors [7213 & 7212] as driver to the S-Video output socket. Likewise the signal D_CVBS is fed through [7606] (6dB amplification) to the rear CVBS cinch socket.

8.3. Digital Board

The Digital Board is based on the highly integrated LSI 'Domino' BGA chip (Ball Grid Array), DMN-8602. This IC has an on-chip ATAPI controller and integrates an analog video encoder, and provides build-in support for non-simultaneous progressive and interlaced video output. A 1394 link layer device is required. The DMN-8602 also has a set of integrated USB Physical Layer Interface.

The board encodes and multiplexes analogue video and digital uncompressed audio (I²S) into an MPEG2 stream. This MPEG2 stream is formatted for recording by the DVD+RW engine. In the playback, the board will decode the MPEG2 video into analogue video. In addition, a DV stream can be received via IEEE 1394 (i-Link), and transformed to MPEG2 format.

8.3.1. Record Mode

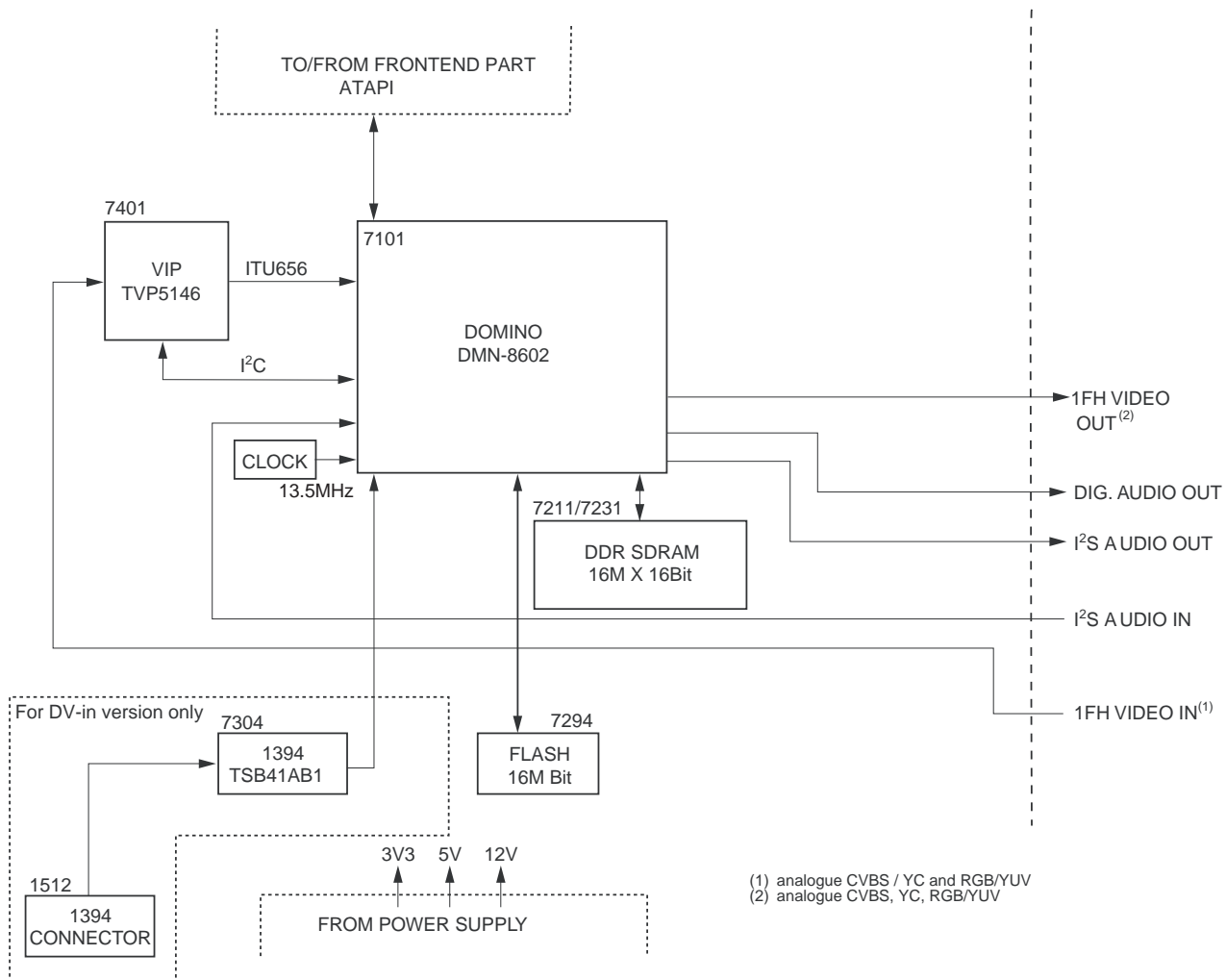


Figure 8-3 Domino block

Video Part

The analogue video input signals CVBS, YC and RGB are routed via the board to connector 1521 and sent to Video Input Processor, TVP5146P [7401].

The digital video input signals from the DV-in on the Front board are routed from connector 1521 via the IEEE 1394 PHY IC [7301] to the Domino chip [7101].

The Video Input Processor encodes the analogue video to digital video stream (CCIR656 format). The output stream, named VID_D (9:0), is then routed to the Domino chip. This IC encodes and decodes the digital video stream into / from MPEG2 format.

Audio Part

I²S audio is sent from the Analog board to the Domino chip via connector 1536.

The Domino chip compresses the I²S audio data into an MPEG1-L2 / AC3 audio stream.

Front-end I²S

The Domino chip interfaces directly to the basic Engine via

ATAPI connector 1571.

It buffers the data streams that are coming from (or going to) the Basic Engine.

In the Domino chip, the video MPEG2 stream and the audio AC3 stream are sent to the basic Engine for recording through ATAPI bus.

8.3.2. Playback mode

During playback, the data from the Basic Engine is going directly to the Domino chip via ATAPI interface. The Domino chip has the following outputs:

- Analogue video CVBS, YC and RGB outputs on connector 1521
- I²S audio (PCM format) on connector 1536
- SPDIF audio (digital audio output) on connector 1536
- Progressive Scan output connector 1522 (Not for European version)

8.3.3. Basic Engine Interface

The Digital board is equipped with an IDE bus (ATAPI) for connecting to the Basic Engine.

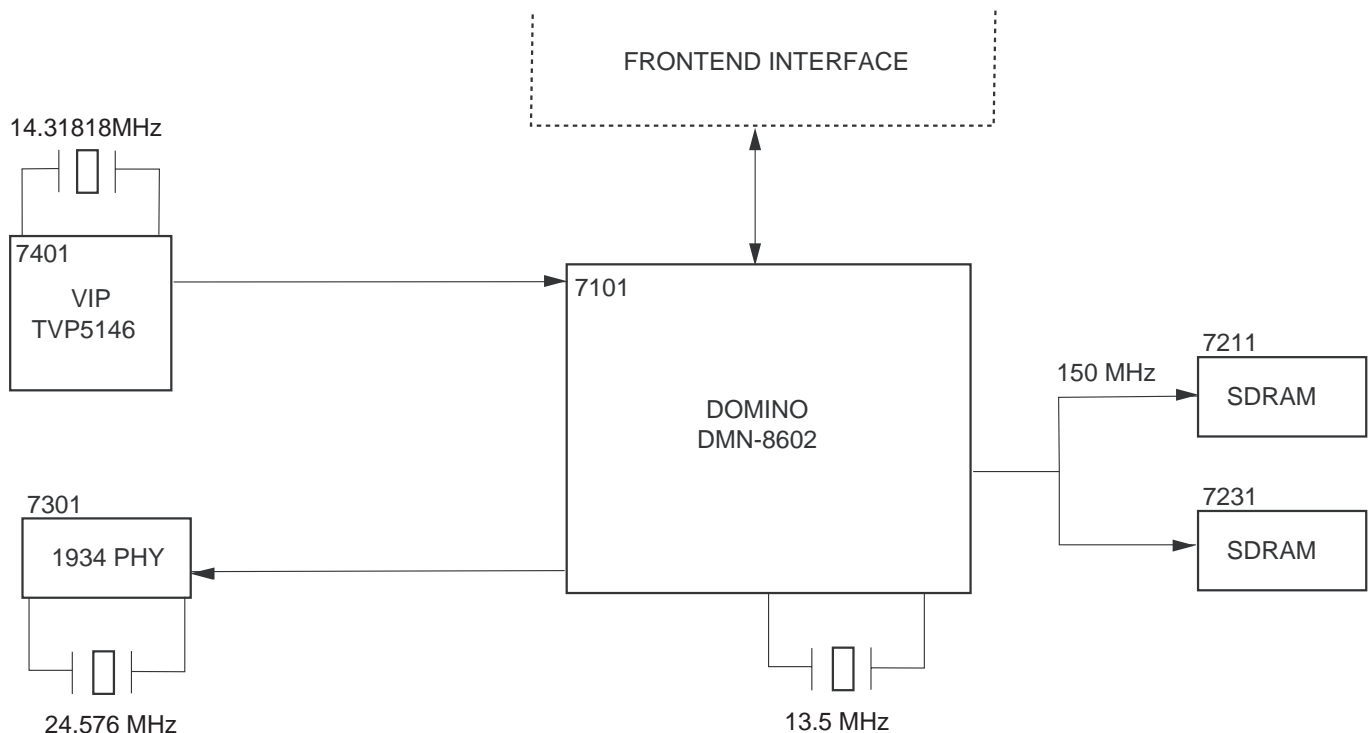
8.3.4. Clock Distribution

Figure 8-4 DIMINO_CLOCK

The Domino chip has a complex system, which is needed to support the processes running at different frequencies such as video decoding, audio decoding or peripheral I/O devices etc. To ensure a synchronous initialization of all the registers and state machines, all the PLLs are switched to their default frequency 27MHz.

Then when the booting control unit is correctly initialized and once it has captured all the booting parameters, it sets the PLLs to its functional frequencies. Thanks to a clock blocking mechanism, the frequency switching is glitch free.

System clocks:

- DMN-8602 (7101, pin E1 and F1): 13.5 MHz provided by the x'tal 1101
- DMN-8602 1394-LINK (7101, pin L1): 49.152MHz provided by 1394-PHY
- TVP5146 (7401, pin 74 and 75): 14.31818MHz provided by x'tal 1461
- SDRAM (7211 and 7231, pin 45 and 46): 150MHz provided by the DMN-8602
- TSB41AB1PHP IEEE 1394 PHY IC (7301, pin 42 and 43): 24.576MHz provided by x'tal 1351

8.3.5. Power Supply

The Digital board is not powered in standby mode. The control signal STBY on the analog board will enable the PSU and power the digital board.

- STBY = Low: the digital board is in powered down standby mode
- STBY = High: the power supply to the digital board is enabled.

The 3V3, +5V and +12V come from the PSU, while the following voltages are generated in the digital board:

- 1.8V core voltage is generated on the board by a 2A switching step down voltage regulator [7521]

- 2.5V supply for the SDRAM is generated by an ultra fast low dropout linear regulator [7515]
- 1.25V DDR termination supply is generated by regulator [7201]

8.3.6. Memory

- FLASH IC7294: this memory contains the boot parameters and application firmware

8.3.7. Reset

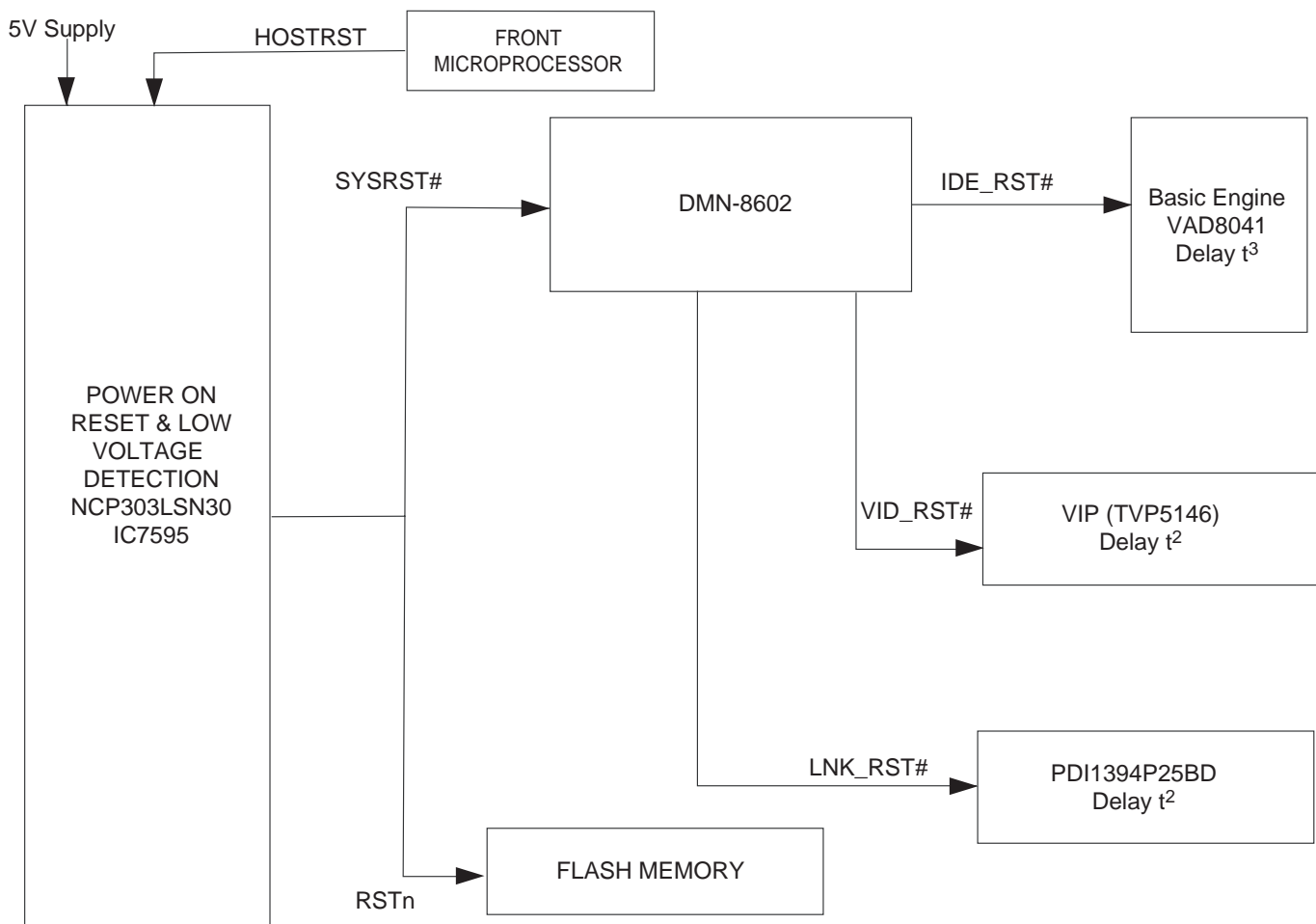


Figure 8-5 DOMINO_RESET

Reset concept Digital board

The reset circuitry [7595] takes care that the different devices on the digital board are boot-up in the correct order. At power on the reset circuitry provides the following resets (delay τ_1):

- SYS_RST# to the Domino chip [7101] and Flash Memory [7294]

The Domino chip then generates other reset signals (delay τ_2) via its GPIOs:

- VID_RST# to reset the VIP [7401]
- LINK_RST# to reset the IEEE1394 DV PHY IC [7301]
- IDE_RST# to reset Basic Engine

8.3.8. I/O Connector

Audio IO Connector (item 136)

The Audio In/Out (AIO) connector is used to interchange digital audio signals between the Analog and Digital board

Video IO Connector (item 1521)

The Video In/Out (VIO) Connector is used to interchange analogue video signals between the Analog and Digital board

8.4 IC Description

8.4.1 Analog Board

IC7421 - TEA1507 - SMPS Control IC

BLOCK DIAGRAM

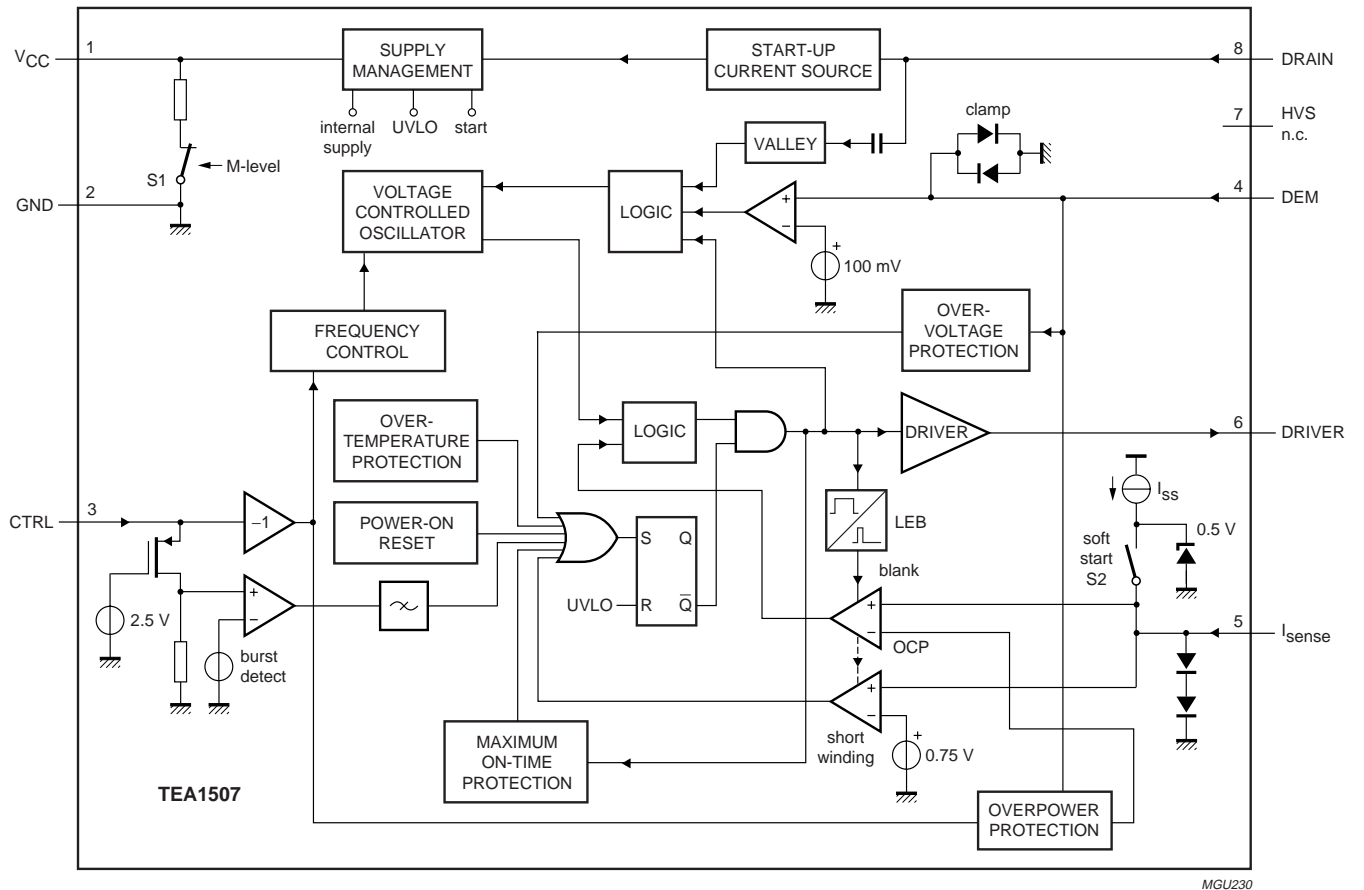


Figure 8-6

PIN DESCRIPTION AND CONFIGURATION

SYMBOL	PIN	DESCRIPTION
V _{CC}	1	supply voltage
GND	2	ground
CTRL	3	control input
DEM	4	input from auxiliary winding for demagnetization timing, OVP and OPP
I _{sense}	5	programmable current sense input
DRIVER	6	gate driver output
HVS	7	high voltage safety spacer, not connected
DRAIN	8	drain of external MOS switch, input for start-up current and valley sensing

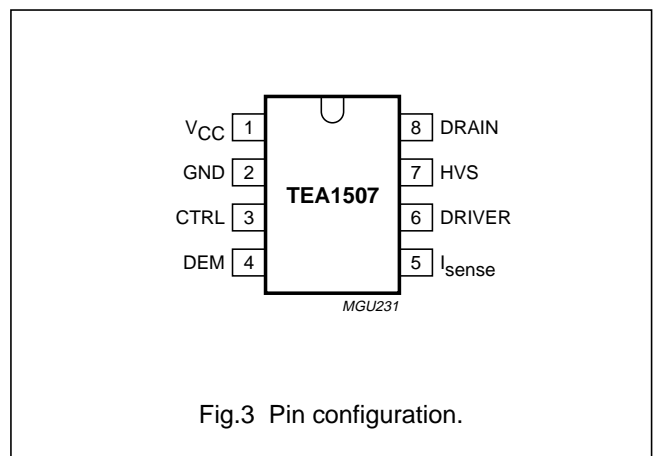


Fig.3 Pin configuration.

IC7500 - MSP34X5G - Multistand Sound Processor Family

BLOCK DIAGRAM

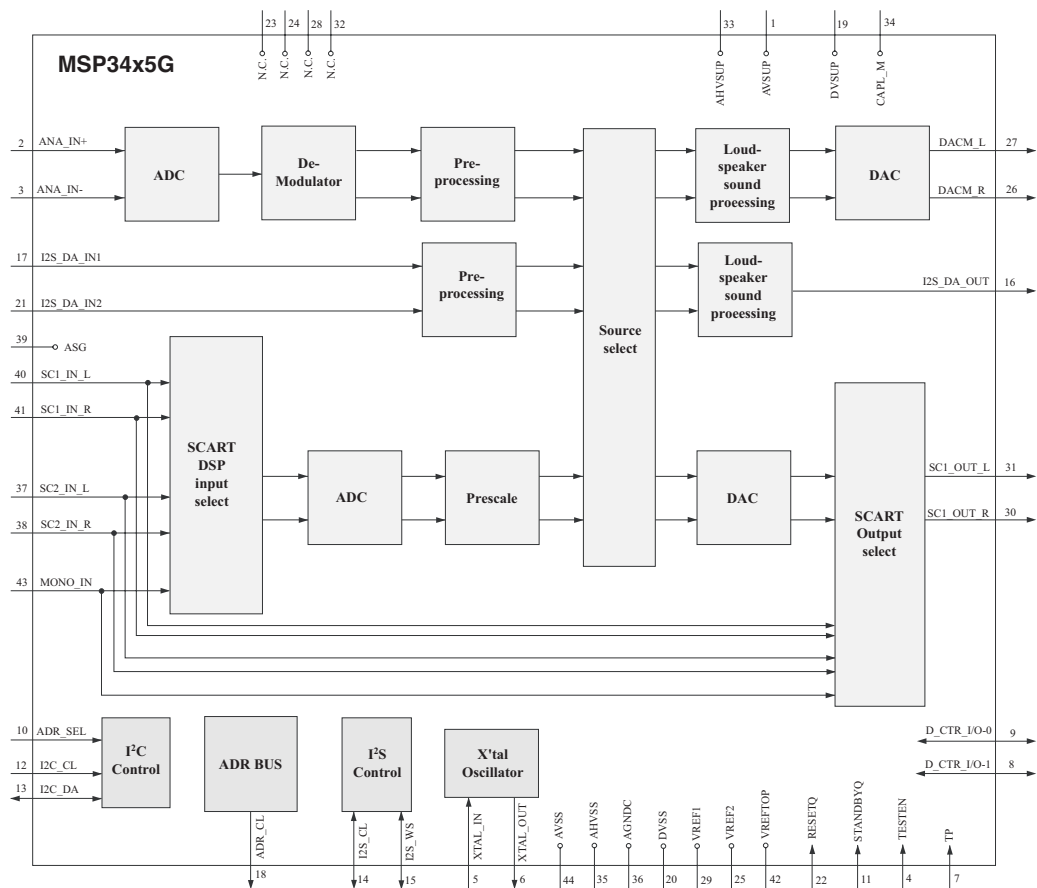
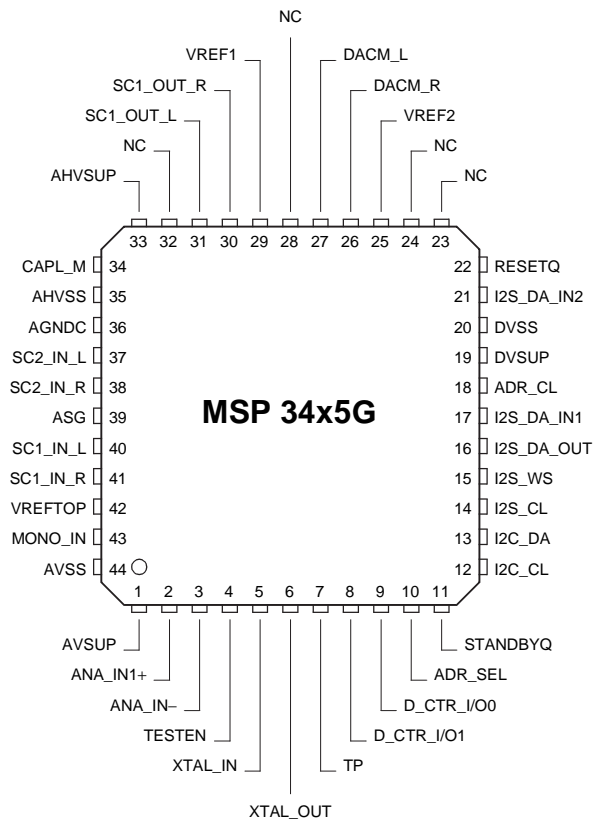


Figure 8-7

PIN CONFIGURATION



PMQFP44 package
Figure 8-8

IC7703 - CS4351 - 192KHz Stereo DAC with 2vrms line-out

BLOCK DIAGRAM

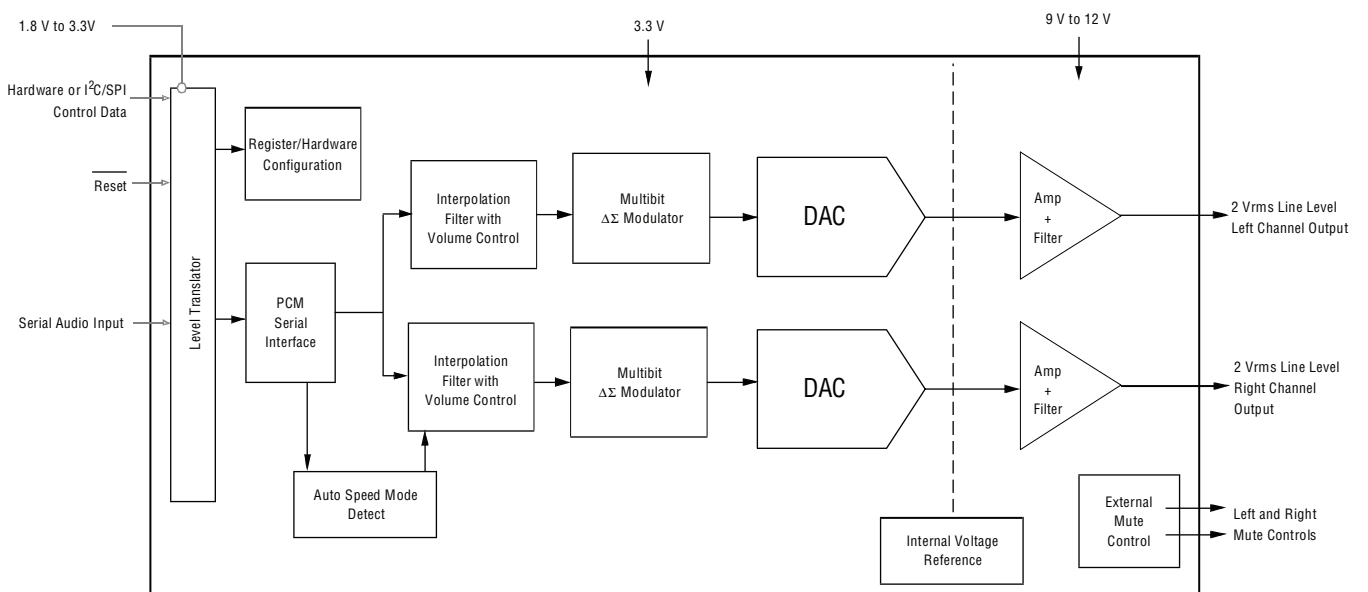
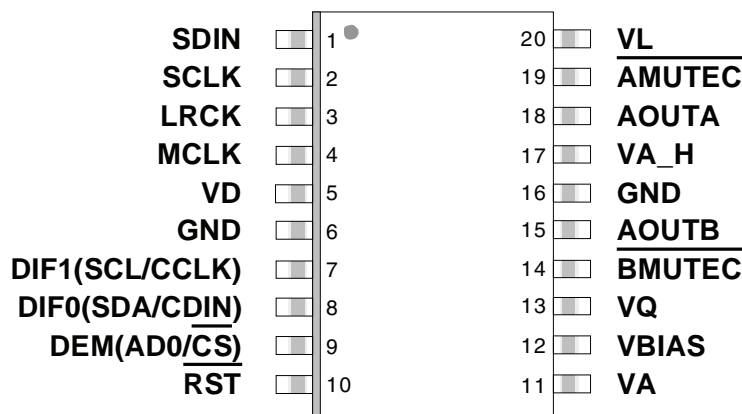


Figure 8-9

PIN DESCRIPTION AND CONFIGURATION



Pin Name	#	Pin Description
SDIN	1	Serial Audio Data Input (<i>Input</i>) - Input for two's complement serial audio data.
SCLK	2	Serial Clock (<i>Input</i>) - Serial clock for the serial audio interface.
LRCK	3	Left / Right Clock (<i>Input</i>) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	4	Master Clock (<i>Input</i>) - Clock source for the delta-sigma modulator and digital filters.
VD	5	Digital Power (<i>Input</i>) - Positive power supply for the digital section.
GND	6	Ground (<i>Input</i>) - Ground reference.
	16	
$\overline{\text{RST}}$	10	Reset (<i>Input</i>) - Powers down device and resets all internal registers to their default settings when enabled.
VA	11	Low Voltage Analog Power (<i>Input</i>) - Positive power supply for the analog section.
VBIAS	12	Positive Voltage Reference (<i>Output</i>) - Positive reference voltage for the internal DAC.
VQ	13	Quiescent Voltage (<i>Output</i>) - Filter connection for internal quiescent voltage.
VA_H	17	High Voltage Analog Power (<i>Input</i>) - Positive power supply for the analog section.
VL	20	Serial Audio Interface Power (<i>Input</i>) - Positive power for the serial audio interface
$\overline{\text{BMUTE C}}$	14	Mute Control (<i>Output</i>) - Control signal for optional mute circuit.
$\overline{\text{AMUTE C}}$	19	
AOUTB	15	Analog Outputs (<i>Output</i>) - The full scale analog line output level is specified in the <i>Analog Characteristics</i> table.
AOUTA	18	
Control Port Definitions		
SCL/CCLK	7	Serial Control Port Clock (<i>Input</i>) - Serial clock for the control port interface.
SDA/CDIN	8	Serial Control Data (<i>Input/Output</i>) - Input/Output for I ² C data. Input for SPI data.
$\overline{\text{AD0/CS}}$	9	Address Bit 0 / Chip Select (<i>Input</i>) - Chip address bit in I ² C Mode. Control Port enable in SPI mode.
Stand-Alone Definitions		
DIF0	8	Digital Interface Format (<i>Input</i>) - Defines the required relationship between the Left Right Clock, Serial Clock, and Serial Audio Data.
DIF1	7	
DEM	9	De-emphasis (<i>Input</i>) - Selects the standard 15 μ s/50 μ s digital de-emphasis filter response for 44.1 kHz sample rates

IC7704 - UDA1361TS - 96KHz Sampling 24-bit stereo audio ADC

BLOCK DIAGRAM

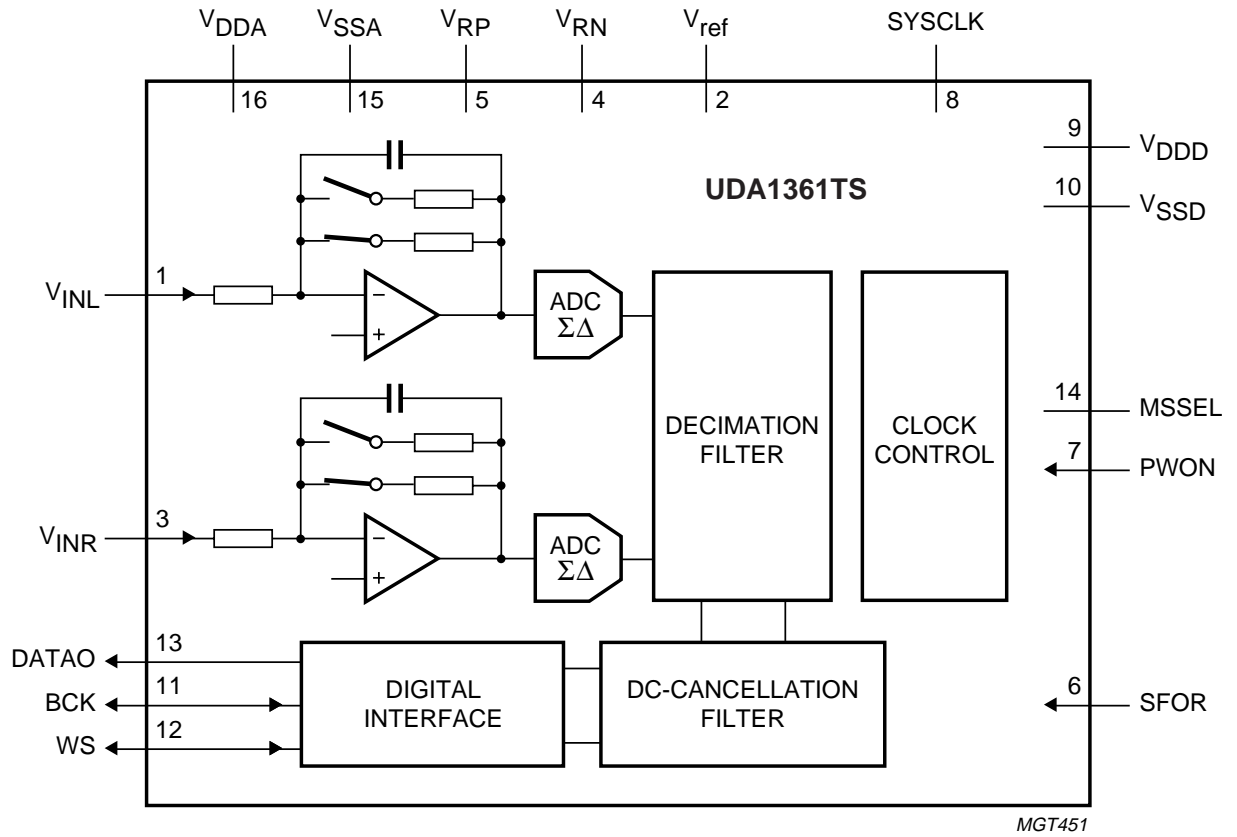
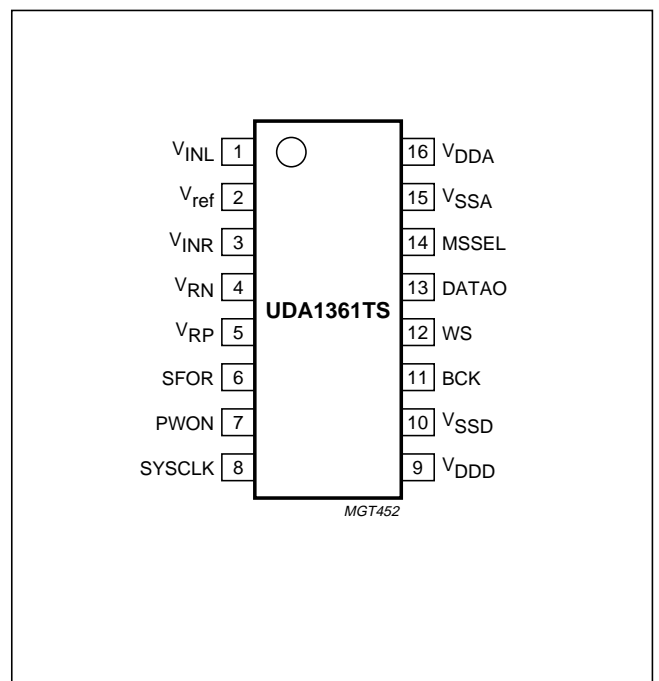


Figure 8-10

PIN DESCRIPTION AND CONFIGURATION

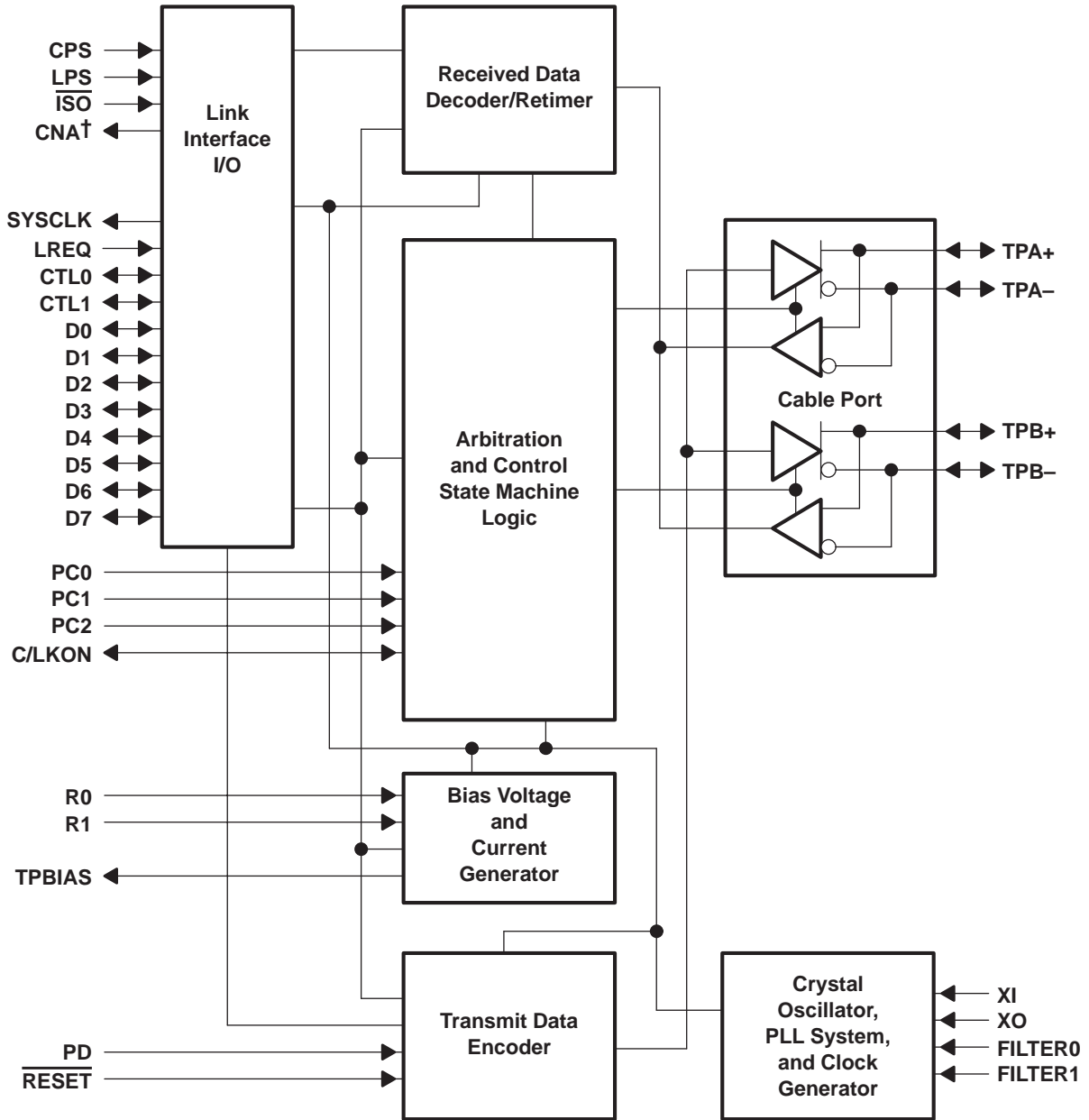
SYMBOL	PIN	DESCRIPTION
V _{INL}	1	left channel input
V _{ref}	2	reference voltage
V _{INR}	3	right channel input
V _{RN}	4	negative reference voltage
V _{RP}	5	positive reference voltage
SFOR	6	data format selection input
PWON	7	power control input
SYSCLK	8	system clock 256, 384, 512 or 768f _s
V _{DDD}	9	digital supply voltage
V _{SSD}	10	digital ground
BCK	11	bit clock input/output
WS	12	word select input/output
DATAO	13	data output
MSSEL	14	master/slave select
V _{SSA}	15	analog ground
V _{DDA}	16	analog supply voltage



8.4.2 Digital Board

IC7301 - TSB41AB1 - IEEE 1394a-2000 one port cable Transceiver/Arbiter

BLOCK DIAGRAM



† CNA output is only available in the 64-pin PAP package

Figure 8-11

PIN CONFIGURATION

PHP package terminal diagram

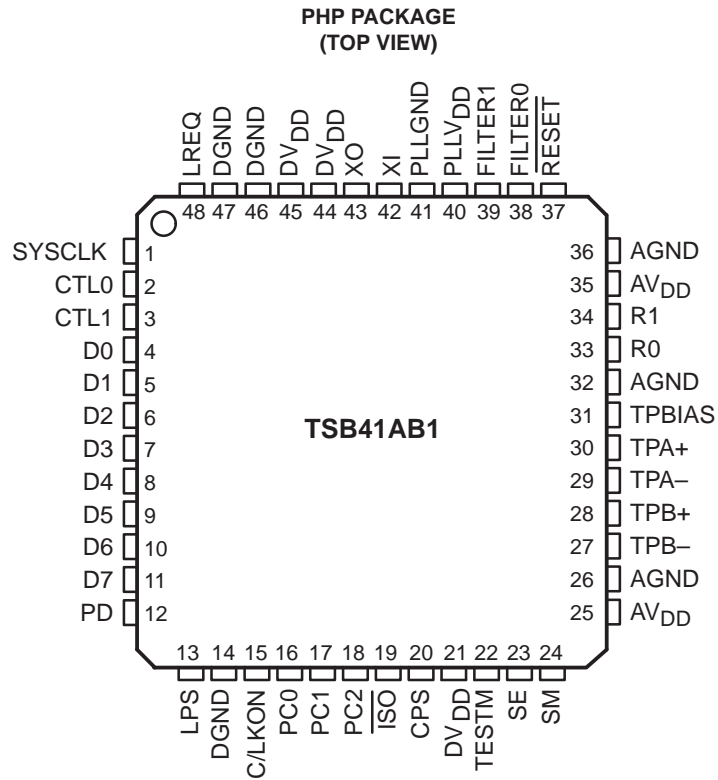


Figure 8-12

PIN DESCRIPTION

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	PHP NO.			
AGND	26, 32, 36	Supply	–	Analog circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
AV _{DD}	25, 35	Supply	–	Analog circuit power terminals. A combination of high frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μ F and 0.001 μ F. Lower frequency 10 μ F filtering capacitors are also recommended. These supply terminals are separated from PLLV _{DD} and DV _{DD} inside the device to provide noise isolation. They should be tied at a low-impedance point on the circuit board.
C/LKON	15	CMOS	I/O	<p>Bus manager contender programming input and link-on output. On hardware reset, this terminal is used to set the default value of the contender status indicated during self-ID. Programming is done by tying the terminal through a 10-kΩ resistor to a high (contender) or low (not contender). The resistor allows the link-on output to override the input. However, it is recommended that this terminal should be programmed low, and that the contender status be set via the C register bit.</p> <p>If the TSB41AB1 is used with an LLC that has a dedicated terminal for monitoring LKON and also setting the contender status, then a 1-kΩ series resistor should be placed on the LKON line between the PHY and LLC to prevent bus contention.</p> <p>Following hardware reset, this terminal is the link-on output, which is used to notify the LLC to power up and become active. The link-on output is a square-wave signal with a period of approximately 163 ns (8 SYSCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is high-impedance.</p> <p>The link-on output is activated if the LLC is inactive (LPS inactive or the LCtrl bit cleared) and when:</p> <ol style="list-style-type: none"> the PHY receives a link-on PHY packet addressed to this node, or the PEI (port-event interrupt) register bit is 1, or any of the CTOI (configuration-time-out interrupt), CPSI (cable-power-status interrupt), or STOI (state-time-out interrupt) register bits are 1 and the RPIE (resuming-port interrupt enable) register bit is also 1. <p>Once activated, the link-on output continues active until the LLC becomes active (both LPS active and the LCtrl bit set). The PHY also deasserts the link-on output when a bus reset occurs unless the link-on output would otherwise be active because one of the interrupt bits is set (that is, the link-on output is active due solely to the reception of a link-on PHY packet).</p> <p>NOTE: If an interrupt condition exists which would otherwise cause the link-on output to be activated if the LLC were inactive, the link-on output is activated when the LLC subsequently becomes inactive.</p>
CNA	N/A	CMOS	O	Cable-not-active output. This terminal is asserted high when there is no incoming bias voltage.
CPS	20	CMOS	I	Cable power status input. This terminal is normally connected to cable power through a 400-k Ω resistor. This circuit drives an internal comparator that is used to detect the presence of cable power. This terminal should be tied directly to DV _{DD} supply if application does not require it to be used.
CTL0 CTL1	2 3	CMOS	I/O	Control I/Os. These bidirectional signals control communication between the TSB41AB1 and the LLC. Bus holders are built into these terminals.
D0 D1 D2 D3 D4 D5 D6 D7	4 5 6 7 8 9 10 11	CMOS	I/O	Data I/Os. These are bidirectional data signals between the TSB41AB1 and the LLC. Bus holders are built into these terminals.

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	PHP NO.			
DGND	14, 46, 47	Supply	–	Digital circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
DVDD	21, 44, 45	Supply	–	Digital circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μ F and 0.001 μ F. Lower frequency 10 μ F filtering capacitors are also recommended. These supply terminals are separated from PLLV _{DD} and AV _{DD} inside the device to provide noise isolation. They should be tied at a low-impedance point on the circuit board.
FILTER0 FILTER1	38 39	CMOS	I/O	PLL filter terminals. These terminals are connected to an external capacitor to form a lag-lead filter required for stable operation of the internal frequency multiplier PLL running from the crystal oscillator. A 0.1 μ F \pm 10% capacitor is the only external component required to complete this filter.
$\overline{\text{ISO}}$	19	CMOS	I	Link interface isolation control input. This terminal controls the operation of output differentiation logic on the CTL and D terminals. If an optional Annex J type isolation barrier is implemented between the TSB41AB1 and LLC, the $\overline{\text{ISO}}$ terminal should be tied low to enable the differentiation logic. If no isolation barrier is implemented (direct connection), or TI bus holder isolation is implemented, the $\overline{\text{ISO}}$ terminal should be tied high to disable the differentiation logic. For additional information refer to TI application note <i>Galvanic Isolation of the IEEE 1394-1995 Serial Bus</i> , SLLA011.
LPS	13	CMOS	I	Link power status input. This terminal monitors the active/power status of the link layer controller and controls the state of the PHY-LLC interface. This terminal should be connected through a 10-k Ω resistor either to the V _{DD} supplying the LLC, or to a pulsed output which is active when the LLC is powered (see Figure 9). A pulsed signal should be used when an isolation barrier exists between the LLC and PHY. (See Figure 10.) The LPS input is considered inactive if it is sampled low by the PHY for more than 2.6 μ s (128 SYSCLK cycles), and is considered active otherwise (that is, asserted steady high or an oscillating signal with a low time less than 2.6 μ s). The LPS input must be high for at least 21 ns to guarantee that a high is observed by the PHY. When the TSB41AB1 detects that LPS is inactive, it places the PHY-LLC interface into a low-power reset state. In the reset state, the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μ s (1280 SYSCLK cycles), the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is placed into the disabled state upon hardware reset. The LLC is considered active only if both the LPS input is active and the LCtrl register bit is set to 1, and is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0.
LREQ	48	CMOS	I	LLC request input. The LLC uses this input to initiate a service request to the TSB41AB1. Bus holder is built into this terminal.
PC0 PC1 PC2	16 17 18	CMOS	I	Power class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying these terminals high or low. Refer to Table 9 for encoding.
PD	12	CMOS	I	Power-down input. A high on this terminal turns off all internal circuitry except the cable-active monitor circuits, which control the CNA output (64-terminal PAP package only). Asserting the PD input high also activates an internal pulldown on the $\overline{\text{RESET}}$ terminal to force a reset of the internal control logic. (PD is provided for legacy compatibility and is not recommended for power management in place of IEEE 1394a-2000 suspend/resume LPS and C/LKON features.)

TERMINAL		TYPE	I/O	DESCRIPTION
NAME	PHP NO.			
PLL _{GND}	41	Supply	–	PLL circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
PLL _{VDD}	40	Supply	–	PLL circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μ F and 0.001 μ F. Lower frequency 10 μ F filtering capacitors are also recommended. This supply terminal is separated from DV _{VDD} and AV _{VDD} inside the device to provide noise isolation. It should be tied at a low-impedance point on the circuit board.
R0 R1	33 34	Bias	–	Current setting resistor terminals. These terminals are connected through an external resistor to set the internal operating currents and cable driver output currents. A resistance of 6.34 k Ω \pm 1.0% is required to meet the IEEE Std 1394-1995 output voltage limits.
$\overline{\text{RESET}}$	37	CMOS	I	Logic reset input. Asserting this terminal low resets the internal logic. An internal pullup resistor to V _{VDD} is provided so only an external delay capacitor is required for proper power-up operation (see <i>power-up reset</i> in the Application Information section). The $\overline{\text{RESET}}$ terminal also incorporates an internal pulldown which is activated when the PD input is asserted high. This input is otherwise a standard logic input, and may also be driven by an open-drain type driver.
SE	23	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41AB1. For normal use this terminal may be tied to GND through a 1-k Ω pulldown resistor or it may be tied to GND directly.
SM	24	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41AB1. For normal use this terminal should be tied to GND.
SYSC _{CLK}	1	CMOS	O	System clock output. Provides a 49.152-MHz clock signal, synchronized with data transfers, to the LLC.
TEST _M	22	CMOS	I	Test control input. This input is used in manufacturing test of the TSB41AB1. For normal use this terminal should be tied to V _{VDD} .
TPA ₊	30	Cable	I/O	Twisted-pair cable A differential signal terminals. Board traces from the pair of positive and negative differential signal terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA _–	29	Cable	I/O	
TPB ₊	28	Cable	I/O	Twisted-pair cable B differential signal terminals. Board traces from the pair of positive and negative differential signal terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB _–	27	Cable	I/O	
TPBIAS	31	Cable	I/O	Twisted-pair bias output. This provides the 1.86 V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection.
XI XO	42 43	Crystal	–	Crystal oscillator inputs. These terminals connect to a 24.576-MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used (see <i>crystal selection</i> in the Application Information section). When an external clock source is used, XI should be the input and XO should be left open, and the clock must be supplied before the device is powered on.

IC7401 - TVP5146PFP - 4x10bit Digital Video Decoder with microvision

BLOCK DIAGRAM

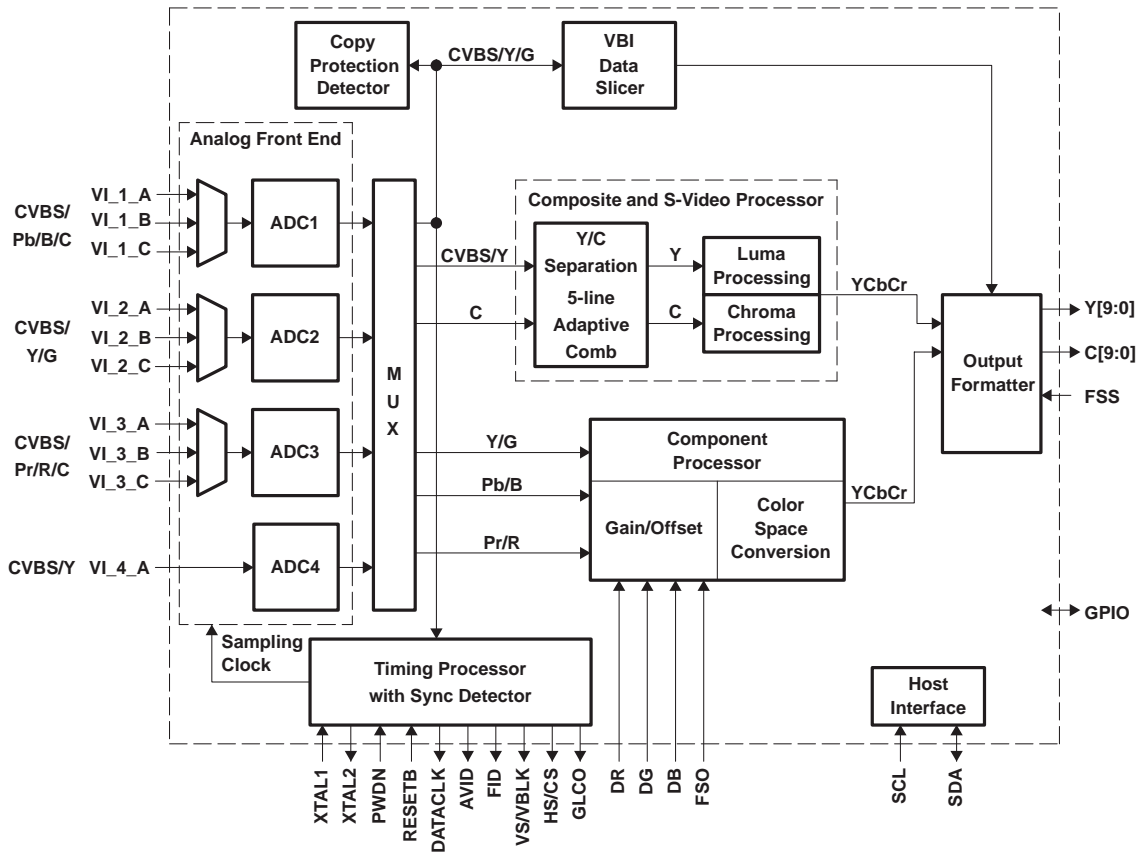


Figure 8-13

PIN CONFIGURATION

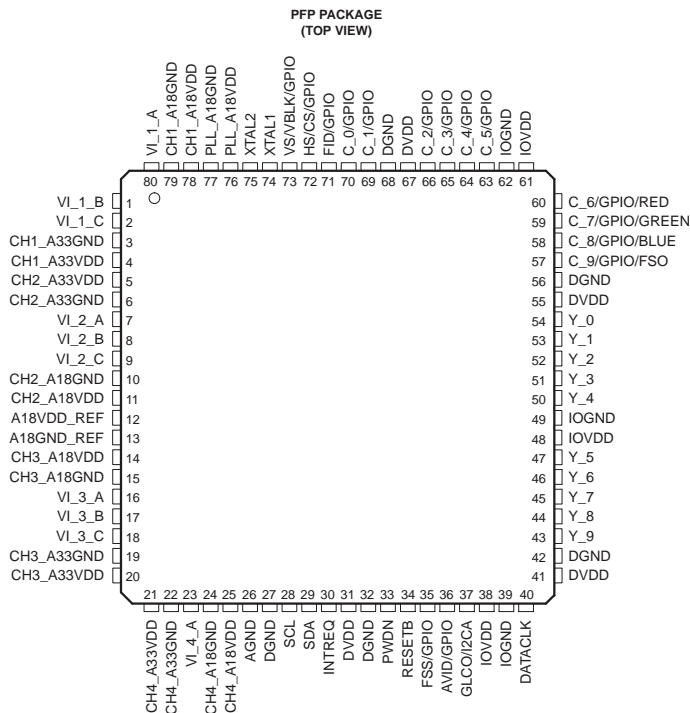


Figure 8-14

PIN DESCRIPTION

TERMINAL NAME	NUMBER	I/O	DESCRIPTION
Analog Video			
VI_1_A	80	I	VI_1_x: Analog video input for CVBS/Pb/B/C VI_2_x: Analog video input for CVBS/Y/G VI_3_x: Analog video input for CVBS/Pr/R/C VI_4_A: Analog video input for CVBS/Y Up to 10 composite, 4 S-video, and 2 composite or 3 component video inputs (or a combination thereof) can be supported. The inputs must be ac-coupled. The recommended coupling capacitor is 0.1 μ F. The possible input configurations are listed in the input select register at I ² C subaddress 00h (see Section 2.11.1).
VI_1_B	1		
VI_1_C	2		
VI_2_A	7		
VI_2_B	8		
VI_2_C	9		
VI_3_A	16		
VI_3_B	17		
VI_3_C	18		
VI_4_A	23		
Clock Signals			
DATACLK	40	O	Line-locked data output clock.
XTAL1	74	I	External clock reference input. It may be connected to an external oscillator with a 1.8-V compatible clock signal or a 14.31818-MHz crystal oscillator.
XTAL2	75	O	External clock reference output. Not connected if XTAL1 is driven by an external single-ended oscillator.
Digital Video			
C[9:0]/ GPIO[9:0]	57, 58, 59, 60, 63, 64, 65, 66, 69, 70	O	Digital video output of CbCr, C[9] is MSB and C[0] is LSB. Unused outputs can be left unconnected. Also, these terminals can be programmable general-purpose I/O. For the 8-bit mode, the two LSBs are ignored.
D_BLUE	58	I	Digital BLUE input from overlay device
D_GREEN	59	I	Digital GREEN input from overlay device
D_RED	60	I	Digital RED input from overlay device
FSO	57	I	Fast-switch overlay between digital RGB and any video
Y[9:0]	43, 44, 45, 46, 47, 50, 51, 52, 53, 54	O	Digital video output of Y/YCbCr, Y[9] is MSB and Y[0] is LSB. For the 8-bit mode, the two LSBs are ignored. Unused outputs can be left unconnected.
Miscellaneous Signals			
FSS/GPIO	35	I/O	Fast-switch (blanking) input. Switching signal between the synchronous component video (YPbPr/RGB) and the composite video input. Programmable general-purpose I/O
GLCO/I2CA	37	I/O	Genlock control output (GLCO). Two Genlock data formats are available: TI format and real time control (RTC) format. During reset, this terminal is an input used to program the I ² C address LSB.
INTREQ	30	O	Interrupt request
PWDN	33	I	Power down input: 1 = Power down 0 = Normal mode
RESETB	34	I	Reset input, active low

TERMINAL NAME	NUMBER	I/O	DESCRIPTION
Host Interface			
SCL	28	I	I ² C clock input
SDA	29	I/O	I ² C data bus
Power Supplies			
AGND	26	I	Analog ground. Connect to analog ground.
A18GND_REF	13	I	Analog 1.8-V return
A18VDD_REF	12	I	Analog power for reference 1.8 V
CH1_A18GND	79	I	Analog 1.8-V return
CH2_A18GND	10		
CH3_A18GND	15		
CH4_A18GND	24		
CH1_A18VDD	78	I	Analog power. Connect to 1.8 V.
CH2_A18VDD	11		
CH3_A18VDD	14		
CH4_A18VDD	25		
CH1_A33GND	3	I	Analog 3.3-V return
CH2_A33GND	6		
CH3_A33GND	19		
CH4_A33GND	22		
CH1_A33VDD	4	I	Analog power. Connect to 3.3 V.
CH2_A33VDD	5		
CH3_A33VDD	20		
CH4_A33VDD	21		
DGND	27, 32, 42, 56, 68	I	Digital return
DVDD	31, 41, 55, 67	I	Digital power. Connect to 1.8 V.
IOGND	39, 49, 62	I	Digital power return
IOVDD	38, 48, 61	I	Digital power. Connect to 3.3 V or less for reduced noise.
PLL_A18GND	77	I	Analog power return
PLL_A18VDD	76	I	Analog power. Connect to 1.8 V.
Sync Signals			
HS/CS/GPIO	72	I/O	Horizontal sync output or digital composite sync output Programmable general-purpose I/O
VS/VBLK/GPIO	73	I/O	Vertical sync output (for modes with dedicated VSYNC) or VBLK output Programmable general-purpose I/O
FID/GPIO	71	I/O	Odd/even field indicator output. This terminal needs a pull-down resistor. Programmable general-purpose I/O
AVID/GPIO	36	I/O	Active video indicator output Programmable general-purpose I/O

IC7501 - TPS2041 - Power Distribution Switches

BLOCK DIAGRAM

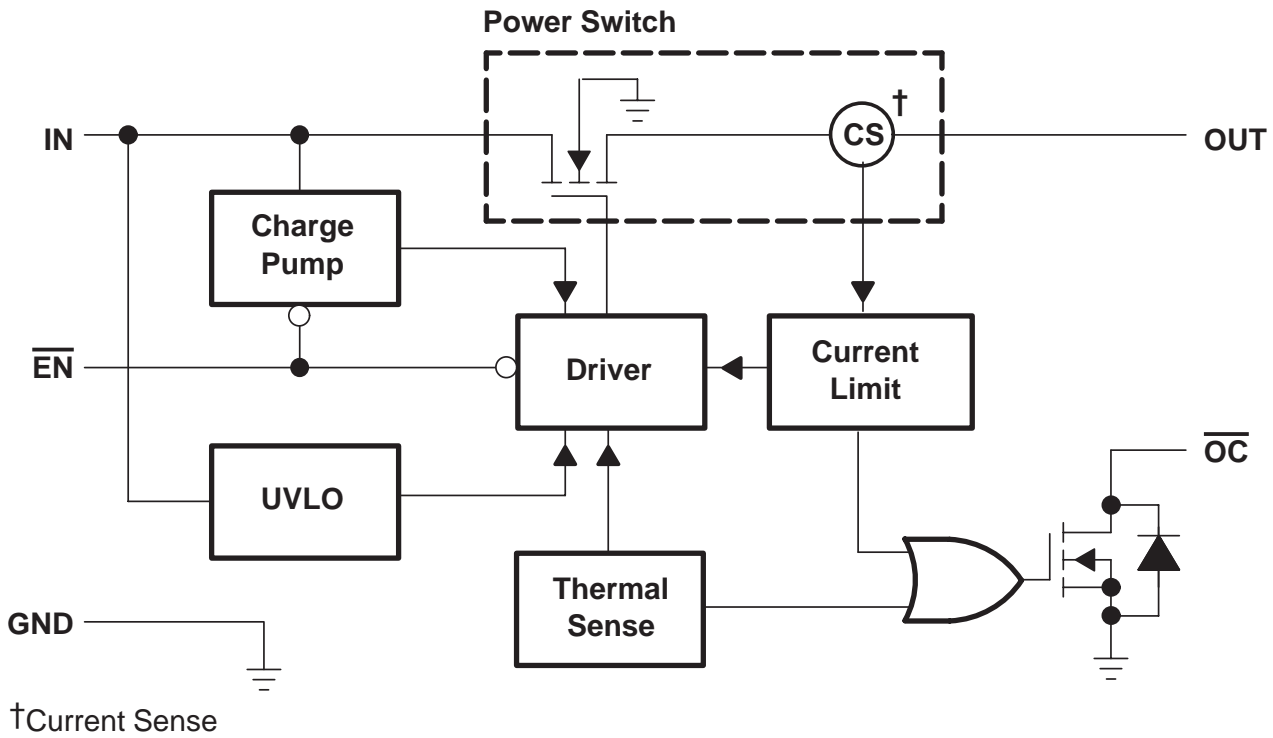


Figure 8-15

PIN CONFIGURATION

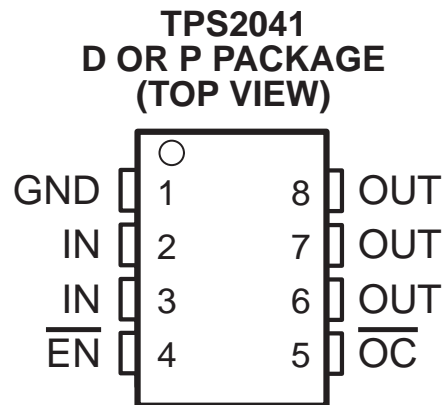
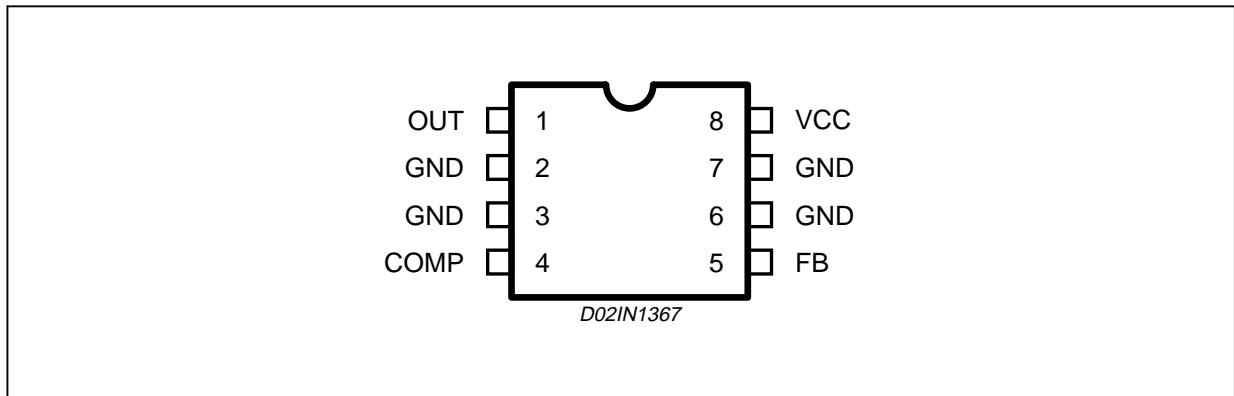


Figure 8-16

PIN DESCRIPTION

NAME	TERMINAL		I/O	DESCRIPTION
	NO.			
	D OR P			
	TPS2041	TPS2051		
$\overline{\text{EN}}$	4	–	I	Enable input. Logic low turns on power switch.
EN	–	4	I	Enable input. Logic high turns on power switch.
GND	1	1	I	Ground
IN	2, 3	2, 3	I	Input voltage
$\overline{\text{OC}}$	5	5	O	Over current. Logic output active low
OUT	6, 7, 8	6, 7, 8	O	Power-switch output

IC7521 - L5972D - 2A Switch Step Down Switching Regulator**PIN DESCRIPTION AND CONFIGURATION****PIN CONNECTION****PIN DESCRIPTION**

N°	Pin	Function
1	OUT	Regulator Output.
2,3,6,7	GND	Ground.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23V. An external resistive divider is required for higher output voltages.
8	VCC	Unregulated DC input voltage.

IC7595 - NCP303 - Voltage Detector Series with Programmable Delay

BLOCK DIAGRAM

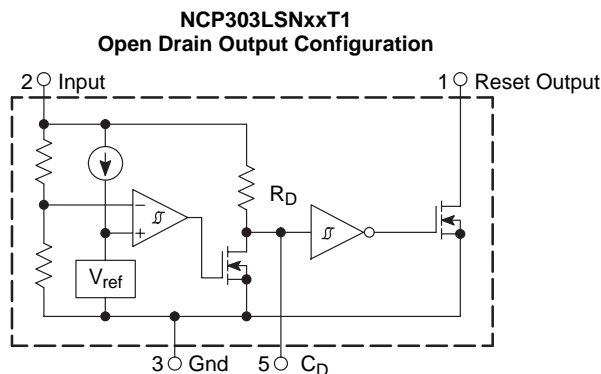
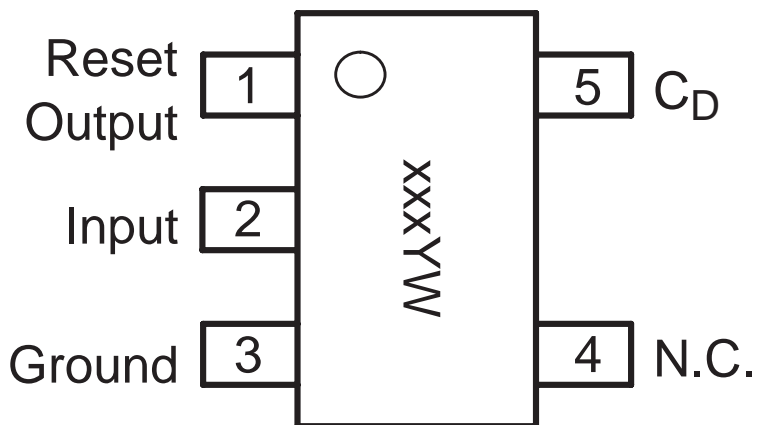


Figure 8-17

PIN DESCRIPTION AND CONFIGURATION

PIN CONNECTIONS AND MARKING DIAGRAM



xxx = 302 or 303
 Y = Year
 W = Work Week

(Top View)

Figure 8-18

Exploded View of the Set

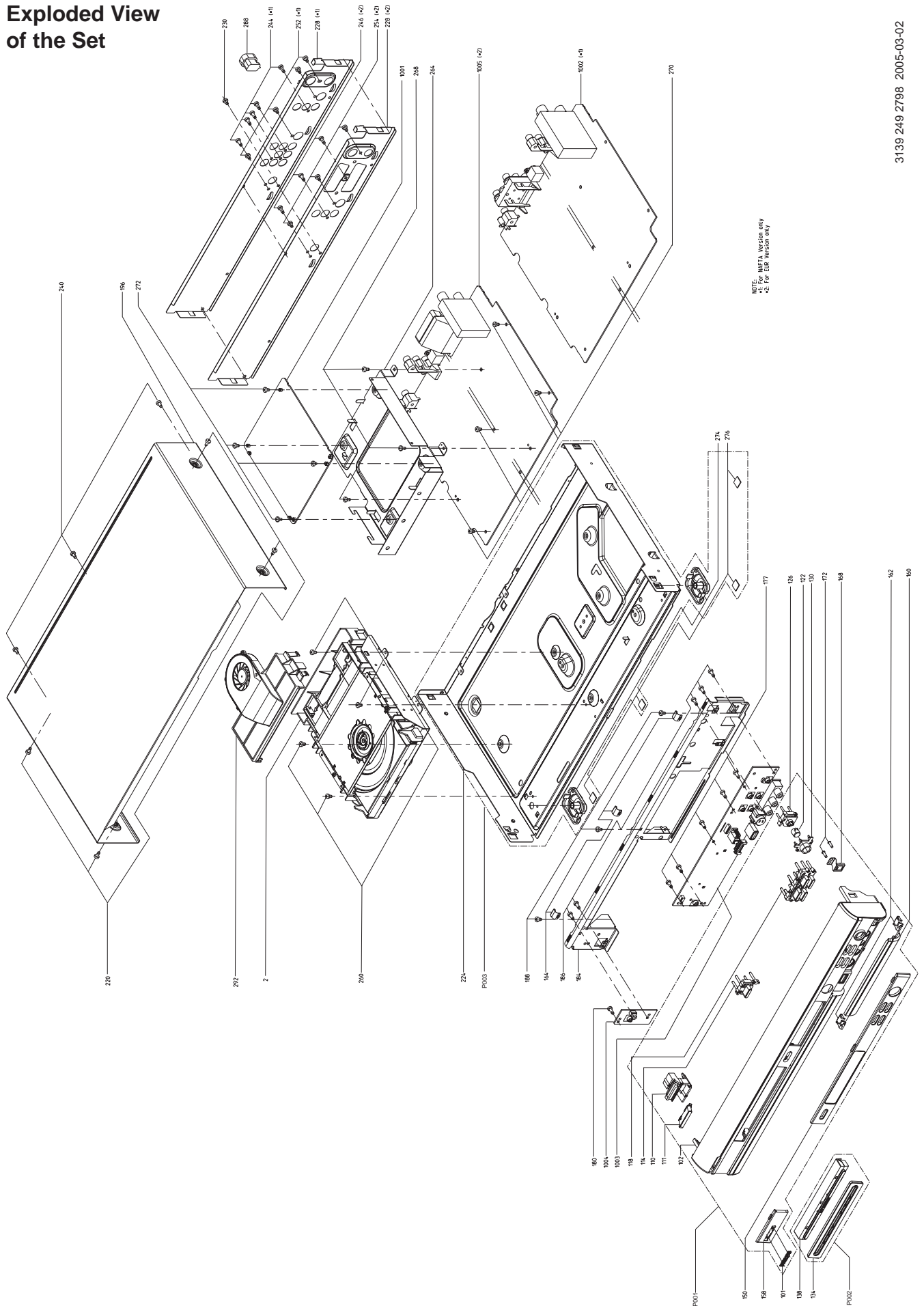


Figure 9-1

Spare Parts List

0002	3139 247 11131	MODULE DRIVE D4.3	
0164	3103 601 20231	SPRING GROUND	
0168	3103 601 20212	SPRING I-LINK	
0196	3139 241 22761	COVER TOP DVDR3305	
0228	3139 241 22791	PLATE REAR EU DVDR3305	
0288	4822 532 60948	BUSH	
0333	2422 549 00607	REMOTE CONTR DVDR3365/EU B	
0333	2422 549 00611	REMOTE CONTR DVDR3355/DVDR3305	
0336	4822 321 11499	△ MAINSCORD	/02, /19, /51 only
0336	2422 070 98236	△ MAINSCORD UK 5A 1M8 VH BK B	/05 only
0342	2422 076 00532	CBLE SCART 1M5 SCART 21P BK B	
0345	4822 320 50377	CONNECT. CABLE PAL	
0901	3143 027 62231	FRONT ASSY DVDR3365	/02, /19, /51 only
0901	3143 027 62261	FRONT ASSY DVDR3365	/05 only
0901	3143 027 62311	FRONT ASSY DVDR3355	/02, /19, /51 only
0901	3143 027 62331	FRONT ASSY DVDR3355	/05 only
0901	3143 027 62681	FRONT ASSY DVDR3305	/02, /19, /51 only
0901	3143 027 62701	FRONT ASSY DVDR3355	/05 only
0910	3143 027 61951	COVER TRAY ASSY DVDR3365	
0910	3143 027 62351	COVER TRAY ASSY DVDR3355	
0910	3143 027 62411	COVER TRAY ASSY DVDR3305	
0920	3143 027 62251	FRAME ASSY	
1001	3139 248 86731	DIGITAL BOARD DVDR3365	/05 only
1001	3139 248 84651	DIGITAL BOARD DVDR3365	/02, /19 only
1001	3139 248 86721	DIGITAL BOARD DVDR3365	/51 only
1001	3139 248 86691	DIGITAL BOARD DVDR3305	/05 only
1001	3139 248 86061	DIGITAL BOARD DVDR3305	/02, /19 only
1001	3139 248 86681	DIGITAL BOARD DVDR3305	/51 only
1001	3139 248 86711	DIGITAL BOARD DVDR3355	/05 only
1001	3139 248 85941	DIGITAL BOARD DVDR3355	/02, /19 only
1001	3139 248 86701	DIGITAL BOARD DVDR3355	/51 only
1003	3139 248 84591	FRONT BOARD DVDR3365	
1003	3139 248 86561	FRONT BOARD DVDR3305	
1003	3139 248 86291	FRONT BOARD DVDR3355	
1004	3139 248 84751	STB BOARD DVDR 3355/DVDR3365	
1004	3139 248 86551	STB BOARD DVDR 3305	
1005	3139 248 84631	ANALOG BOARD DVDR3355/DVDR3365	
1005	3139 248 86571	ANALOG BOARD DVDR3305	
8002	3139 110 35631	FFC FOIL 22P/180/22P BD 1MMP	
8003	3139 241 01081	FFC FOIL 20P/140/20P BD 1MMP	
8004	3139 241 00241	FFC FOIL 30P/140/30P BD 1MMP	
8007	3139 241 00591	CBLE HR 04P/220/04P LOADER SUP	
8008	3139 241 01011	FFC FOIL 14P/180/14P BD 1MMP	
8010	3139 241 00921	CBLE IDE 40P/280/40P IDE UL	
8011	2422 076 00676	CBLE IEEE1394 DVDR3355/DVDR3365	

10. REVISION LIST

Version 1.0

* Original Release

Version 1.1

* Add missing Exploded View drawing